ROM-7421
A101-3

#IP ID

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Title: Title Page

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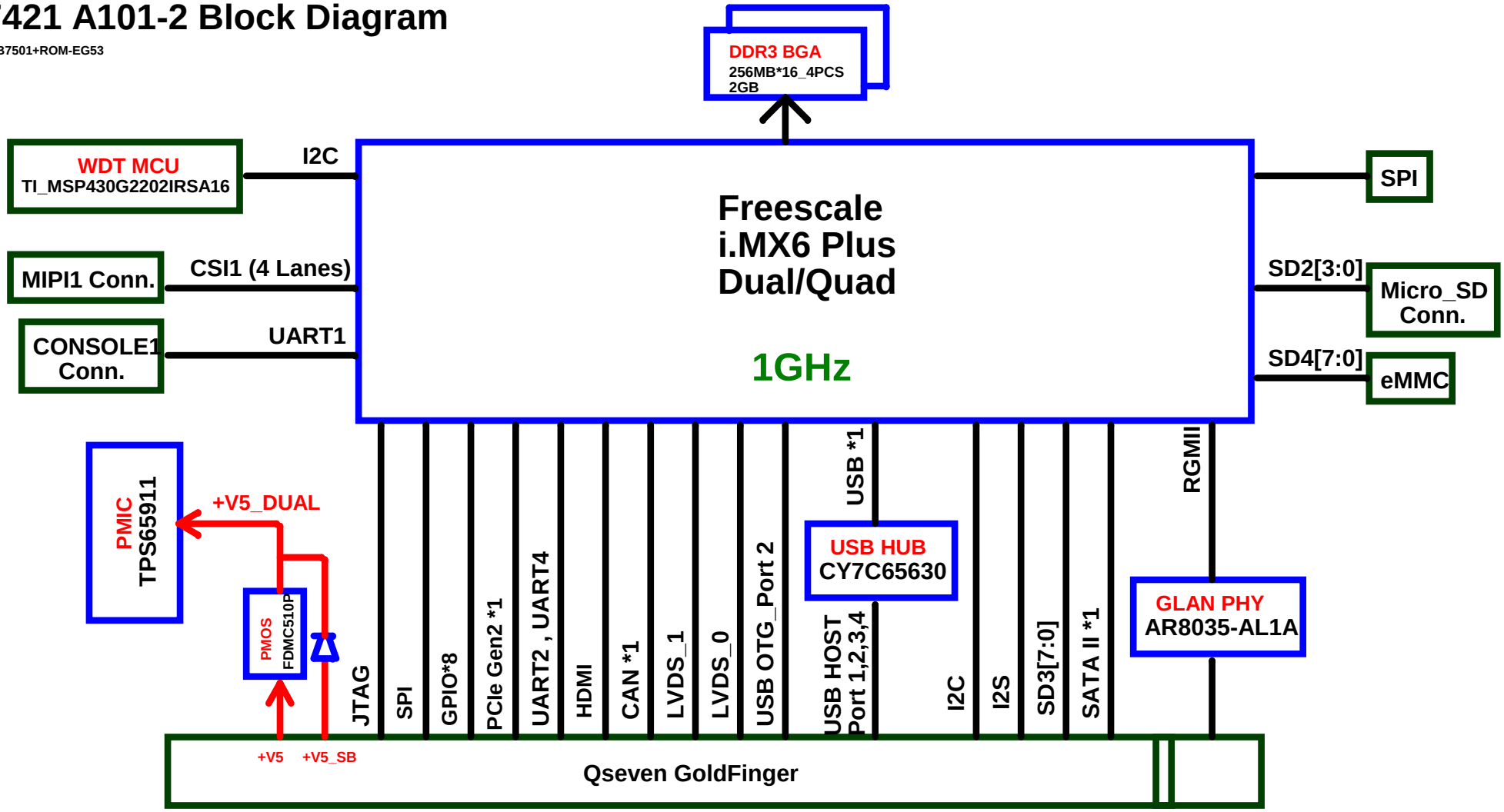
ROM-7421 A101-2 Block Diagram

Test configuration:
ROM-7421+ROM-DB7501+ROM-EG53



BOM_Value	96 P/N	TEMP	ARM	MEM	eMMC	WDT	OTG	USB_HOST	LAN	MicroSD	MIPI
Part_Number_Value		0~60	MCIMX6DP6AVT1AA (Dual)	128Mx16 x4pcs	4GB	V	V	4	AR8035	V	V
Part_Number_ND1G14	9696O74200E	0~60	MCIMX6DP5EYM1AA (Dual)	128Mx16 x4pcs	4GB	V	V	4	AR8035	V	V
Part_Number_NQ1G24	9696O74210E	0~60	MCIMX6QP5EYM1AA (Quad)	256Mx16 x4pcs	4GB	V	V	4	AR8035	V	V
Part_Number_WQ1G28		-40~85	Quad Core	256Mx16 x4pcs	8GB	V	V	4	AR8035	V	V

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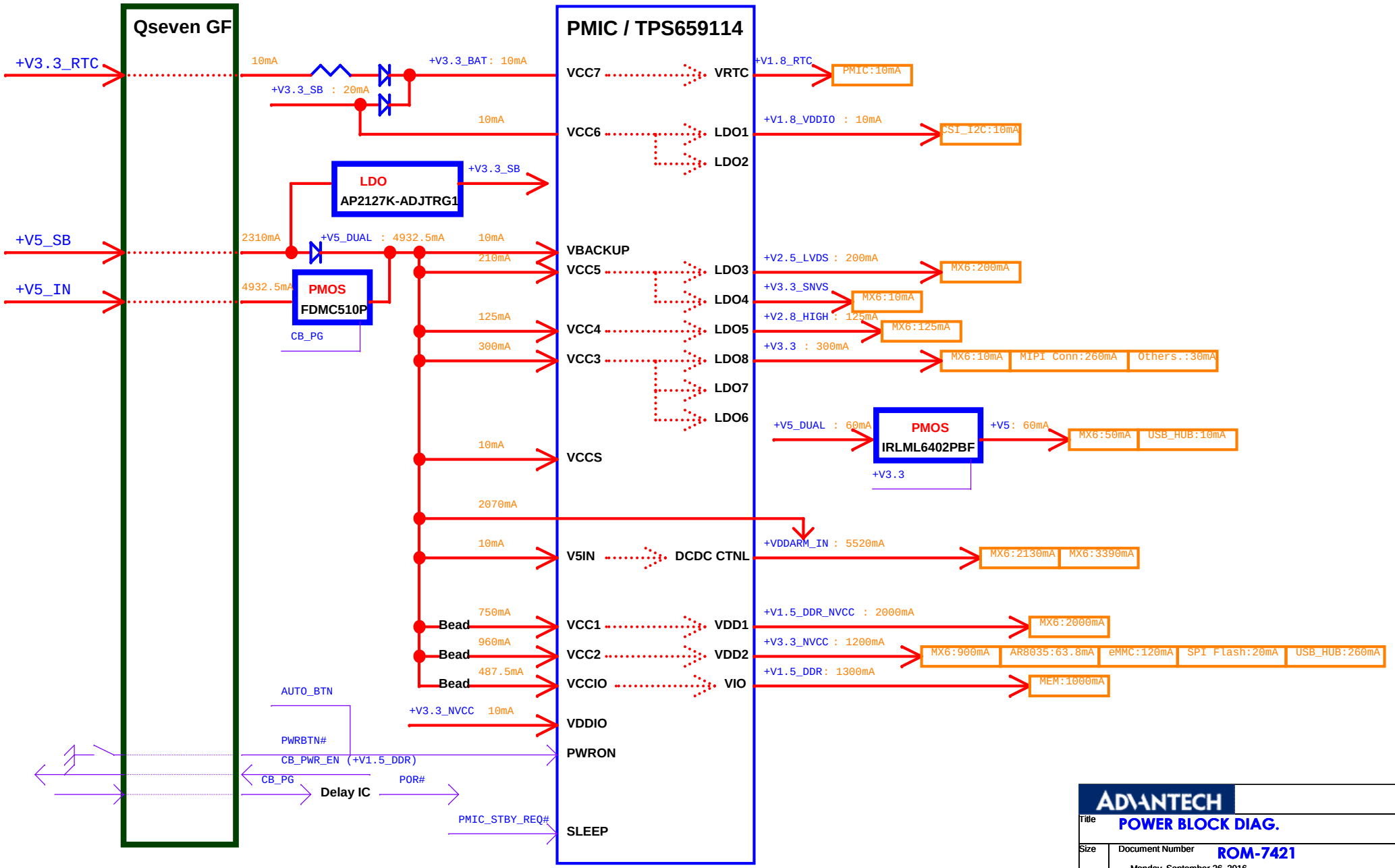
Power Delivery



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Title	POWER BLOCK DIAG.	
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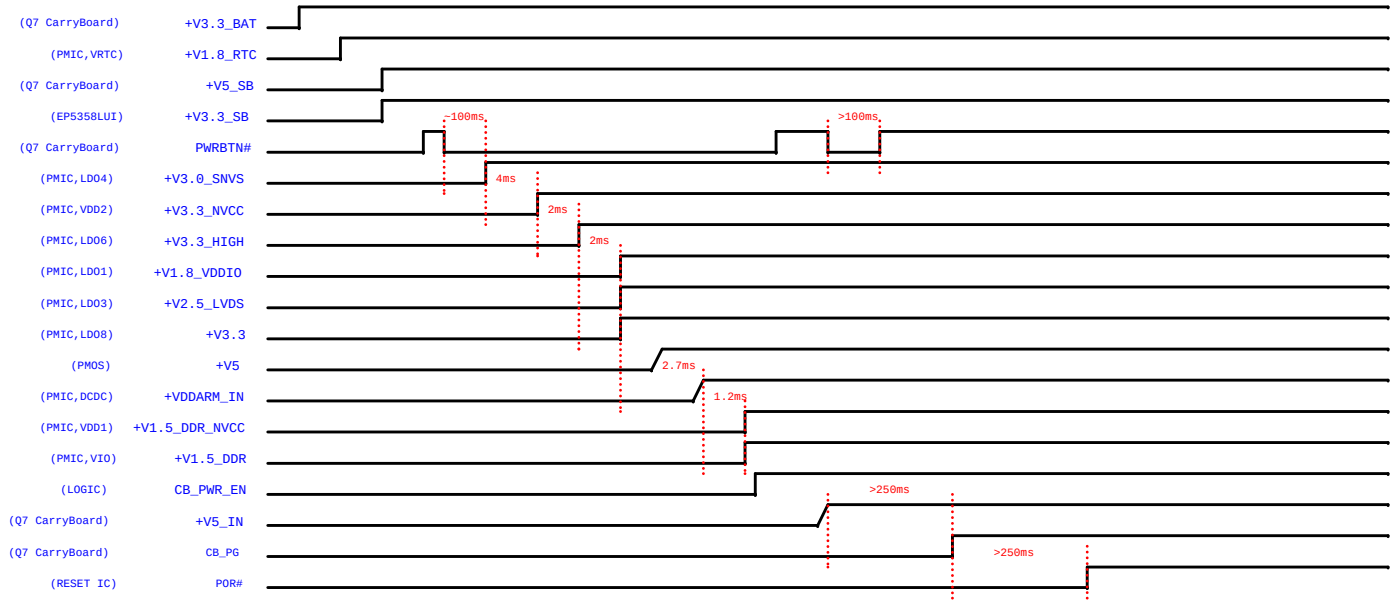
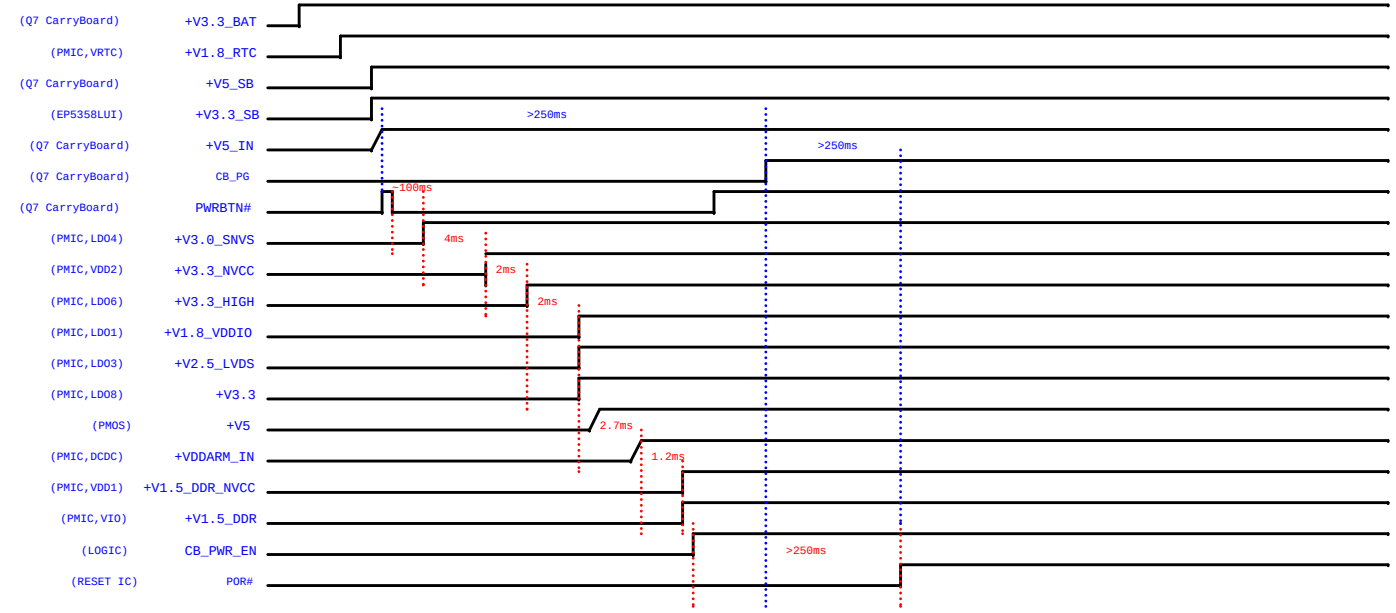
Power Sequence

ATX Mode :



AT Mode :



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Title	POWER ON SEQ.	
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PIN MUX TABLES

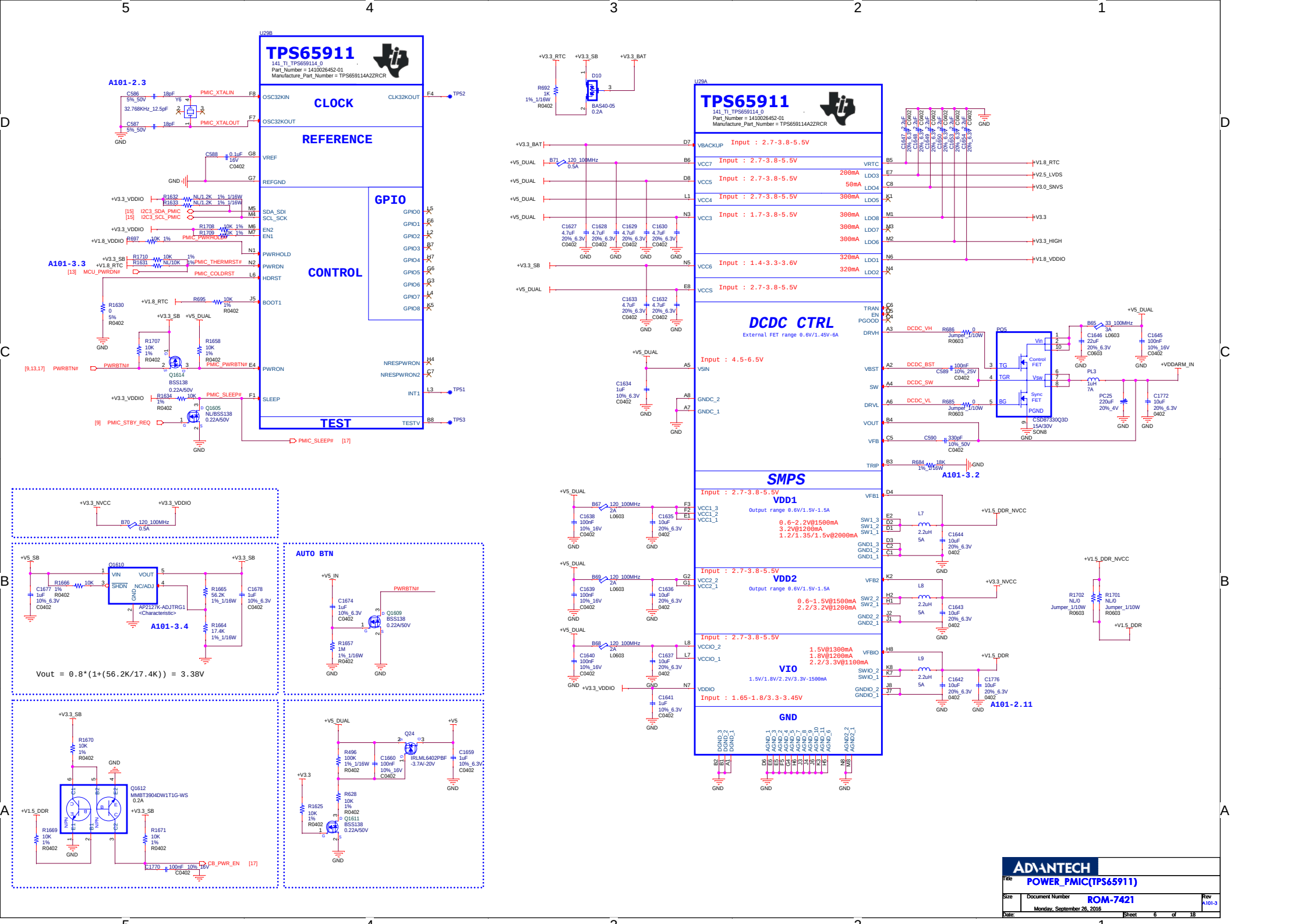
Pad #	Pad name	Ball	Power Group	Default Mode (Reset Mode)	ALT mode Configured for usecase - valid only if pad is allocated (LOCK in previous column)	ROM-7421 NetName
PAD1	SD2_DAT1	E20	SD2	ALT5	ALT0	SD2_MICRO_DATA1
PAD2	SD2_DAT2	A23	SD2	ALT5	ALT0	SD2_MICRO_DATA2
PAD4	SD2_DAT0	A22	SD2	ALT5	ALT0	SD2_MICRO_DATA0
PAD6	RGMII_TXC	D21	RGMII	ALT5	ALT1	RGMII_TXCLK
PAD7	RGMII_TD0	C22	RGMII	ALT5	ALT1	RGMII_TXD0
PAD10	RGMII_TD1	F20	RGMII	ALT5	ALT1	RGMII_TXD1
PAD11	RGMII_TD2	E21	RGMII	ALT5	ALT1	RGMII_TXD2
PAD12	RGMII_TD3	A24	RGMII	ALT5	ALT1	RGMII_TXD3
PAD13	RGMII_RX_CTL	D22	RGMII	ALT5	ALT1	RGMII_RXCTL
PAD16	RGMII_RD0	C24	RGMII	ALT5	ALT1	RGMII_RXD0
PAD17	RGMII_TX_CTL	C23	RGMII	ALT5	ALT1	RGMII_TXCTL
PAD18	RGMII_RD1	B23	RGMII	ALT5	ALT1	RGMII_RXD1
PAD19	RGMII_RD2	B24	RGMII	ALT5	ALT1	RGMII_RXD2
PAD22	RGMII_RD3	D23	RGMII	ALT5	ALT1	RGMII_RXD3
PAD23	RGMII_RXC	B25	RGMII	ALT5	ALT1	RGMII_RXCLK
PAD25	EIM_A25	H19	WEIM_SEC	ALT0	ALT5	GPIO_Q7-8
PAD26	EIM_EB2	E22	WEIM_SEC	ALT5	ALT0	EIM_EB2
PAD28	EIM_D16	C25	WEIM_SEC	ALT5	ALT1	CSPI1_CLK
PAD29	EIM_D17	F21	WEIM_SEC	ALT5	ALT1	CSPI1_MISO
PAD30	EIM_D18	D24	WEIM_SEC	ALT5	ALT1	CSPI1_MOSI
PAD31	EIM_D19	G21	WEIM_SEC	ALT5	ALT1	CSPI1_CS1
PAD32	EIM_D20	G20	WEIM_SEC	ALT5	ALT0	PCIE_PWR_EN
PAD34	EIM_D21	H20	WEIM_SEC	ALT5	ALT5	USB_OTG_OC
PAD35	EIM_D22	E23	WEIM_SEC	ALT5	ALT0	USB_OTG_PWR_EN
PAD36	EIM_D23	D25	WEIM_SEC	ALT5	ALT5	USB_OTG_PWREN#
PAD37	EIM_EB3	F23	WEIM_SEC	ALT5	ALT0	EIM_EB3
PAD38	EIM_D24	F22	WEIM_SEC	ALT5	ALT0	EIM_D24
PAD40	EIM_D25	G22	WEIM_SEC	ALT5	ALT0	EIM_D25
PAD41	EIM_D26	E24	WEIM_SEC	ALT5	ALT4	UART2_TXD
PAD42	EIM_D27	E25	WEIM_SEC	ALT5	ALT4	UART2_RXD
PAD43	EIM_D28	G23	WEIM_SEC	ALT5	ALT4	UART2_CTS
PAD44	EIM_D29	J19	WEIM_SEC	ALT5	ALT4	UART2_RTS
PAD46	EIM_D30	J20	WEIM_SEC	ALT5	ALT5	BRD_ID1
PAD47	EIM_D31	H21	WEIM_SEC	ALT5	ALT5	BRD_ID0
PAD49	EIM_A24	F25	WEIM_MAIN__0	ALT0	ALT0	EIM_A24
PAD50	EIM_A23	J21	WEIM_MAIN__0	ALT0	ALT0	EIM_A23
PAD51	EIM_A22	F24	WEIM_MAIN__0	ALT0	ALT0	EIM_A22
PAD53	EIM_A21	H23	WEIM_MAIN__0	ALT0	ALT0	EIM_A21
PAD54	EIM_A20	H22	WEIM_MAIN__0	ALT0	ALT0	EIM_A20
PAD55	EIM_A19	G25	WEIM_MAIN__0	ALT0	ALT0	EIM_A19
PAD56	EIM_A18	J22	WEIM_MAIN__0	ALT0	ALT0	EIM_A18
PAD57	EIM_A17	G24	WEIM_MAIN__0	ALT0	ALT0	EIM_A17
PAD59	EIM_A16	H25	WEIM_MAIN__0	ALT0	ALT0	EIM_A16
PAD60	EIM_CS0	H24	WEIM_MAIN__0	ALT0	ALT5	GPIO_Q7-6
PAD61	EIM_CS1	J23	WEIM_MAIN__0	ALT0	ALT5	GPIO_Q7-7
PAD62	EIM_OE	J24	WEIM_MAIN__0	ALT0	ALT5	GPIO_Q7-5
PAD63	EIM_RW	K20	WEIM_MAIN__0	ALT0	ALT0	EIM_RW
PAD65	EIM_LBA	K22	WEIM_MAIN__0	ALT0	ALT0	EIM_LBA
PAD67	EIM_EB0	K21	WEIM_MAIN__1	ALT0	ALT0	EIM_EB0
PAD68	EIM_EB1	K23	WEIM_MAIN__1	ALT0	ALT0	EIM_EB1
PAD69	EIM_DA0	L20	WEIM_MAIN__1	ALT0	ALT0	EIM_DA0
PAD70	EIM_DA1	J25	WEIM_MAIN__1	ALT0	ALT0	EIM_DA1
PAD72	EIM_DA2	L21	WEIM_MAIN__1	ALT0	ALT0	EIM_DA2
PAD73	EIM_DA3	K24	WEIM_MAIN__1	ALT0	ALT0	EIM_DA3
PAD74	EIM_DA4	L22	WEIM_MAIN__1	ALT0	ALT0	EIM_DA4
PAD75	EIM_DA5	L23	WEIM_MAIN__1	ALT0	ALT0	EIM_DA5
PAD76	EIM_DA6	K25	WEIM_MAIN__1	ALT0	ALT0	EIM_DA6
PAD78	EIM_DA7	L25	WEIM_MAIN__1	ALT0	ALT0	EIM_DA7
PAD79	EIM_DA8	L24	WEIM_MAIN__1	ALT0	ALT0	EIM_DA8
PAD80	EIM_DA9	M21	WEIM_MAIN__1	ALT0	ALT0	EIM_DA9
PAD81	EIM_DA10	M22	WEIM_MAIN__1	ALT0	ALT0	EIM_DA10
PAD82	EIM_DA11	M20	WEIM_MAIN__1	ALT0	ALT0	EIM_DA11
PAD84	EIM_DA12	M24	WEIM_MAIN__1	ALT0	ALT0	EIM_DA12
PAD85	EIM_DA13	M23	WEIM_MAIN__1	ALT0	ALT0	EIM_DA13
PAD86	EIM_DA14	N23	WEIM_MAIN__1	ALT0	ALT0	EIM_DA14
PAD87	EIM_DA15	N24	WEIM_MAIN__1	ALT0	ALT0	EIM_DA15
PAD88	EIM_WAIT	M25	WEIM_MAIN__1	ALT0	ALT0	EIM_WAIT
PAD90	EIM_BCLK	N22	WEIM_MAIN__1	ALT0	ALT0	EIM_BCLK
PAD92	DI0_DISP_CLK	N19	IPU_LCD	ALT5	ALT0	N/A
PAD93	DI0_PIN15	N21	IPU_LCD	ALT5	ALT0	N/A
PAD94	DI0_PIN2	N25	IPU_LCD	ALT5	ALT0	N/A
PAD95	DI0_PIN3	N20	IPU_LCD	ALT5	ALT0	N/A
PAD97	DI0_PIN4	P25	IPU_LCD	ALT5	ALT5	N/A
PAD98	DISP0_DAT0	P24	IPU_LCD	ALT5	ALT0	N/A
PAD99	DISP0_DAT1	P22	IPU_LCD	ALT5	ALT0	N/A
PAD100	DISP0_DAT2	P23	IPU_LCD	ALT5	ALT0	N/A
PAD101	DISP0_DAT3	P21	IPU_LCD	ALT5	ALT0	N/A
PAD103	DISP0_DAT4	P20	IPU_LCD	ALT5	ALT0	N/A
PAD104	DISP0_DAT5	R25	IPU_LCD	ALT5	ALT0	N/A
PAD105	DISP0_DAT6	R23	IPU_LCD	ALT5	ALT0	N/A
PAD106	DISP0_DAT7	R24	IPU_LCD	ALT5	ALT0	N/A
PAD107	DISP0_DAT8	R22	IPU_LCD	ALT5	ALT0	N/A
PAD109	DISP0_DAT9	T25	IPU_LCD	ALT5	ALT0	N/A
PAD110	DISP0_DAT10	R21	IPU_LCD	ALT5	ALT0	N/A
PAD111	DISP0_DAT11	T23	IPU_LCD	ALT5	ALT0	N/A
PAD112	DISP0_DAT12	T24	IPU_LCD	ALT5	ALT0	N/A
PAD113	DISP0_DAT13	R20	IPU_LCD	ALT5	ALT0	N/A
PAD115	DISP0_DAT14	U25	IPU_LCD	ALT5	ALT0	N/A
PAD116	DISP0_DAT15	T22	IPU_LCD	ALT5	ALT0	N/A
PAD117	DISP0_DAT16	T21	IPU_LCD	ALT5	ALT0	N/A
PAD118	DISP0_DAT17	U24	IPU_LCD	ALT5	ALT0	N/A
PAD119	DISP0_DAT18	V25	IPU_LCD	ALT5	ALT0	N/A
PAD121	DISP0_DAT19	U23	IPU_LCD	ALT5	ALT0	N/A
PAD122	DISP0_DAT20	U22	IPU_LCD	ALT5	ALT0	N/A
PAD123	DISP0_DAT21	T20	IPU_LCD	ALT5	ALT0	N/A
PAD124	DISP0_DAT22	V24	IPU_LCD	ALT5	ALT0	N/A
PAD125	DISP0_DAT23	W24	IPU_LCD	ALT5	ALT0	N/A
PAD128	ENET_MDIO	V23	ENET	ALT5	ALT1	RGMII_MDIO
PAD129	ENET_REF_CLK	V22	ENET	ALT5	ALT1	ENET_REFCLK
PAD130	ENET_RX_ER	W23	ENET	ALT5	ALT0	USB_OTG_ID
PAD131	ENET_CRS_DV	U21	ENET	ALT5	ALT5	RGMII_RST#
PAD132	ENET_RXD1	W22	ENET	ALT5	ALT5	RGMII_INT
PAD134	ENET_RXD0	W21	ENET	ALT5	ALT5	N/A
PAD135	ENET_TX_EN	V21	ENET	ALT5	ALT5	ETH_WOL_INT
PAD136	ENET_TXD1	W20	ENET	ALT5	ALT5	THRM_DOWN#
PAD137	ENET_TXD0	U20	ENET	ALT5	ALT5	PCIE_WAKE#
PAD138	ENET_MDC	V20	ENET	ALT5	ALT1	RGMII_MDC
PAD321	KEY_COL0	W5	GPIO	ALT5	ALT5	N/A
PAD322	KEY_ROW0	V6	GPIO	ALT5	ALT5	N/A
PAD324	KEY_COL1	U7	GPIO	ALT5	ALT5	N/A
PAD325	KEY_ROW1	U6	GPIO	ALT5	ALT5	N/A
PAD326	KEY_COL2	W6	GPIO	ALT5	ALT5	N/A
PAD328	KEY_ROW2	W4	GPIO	ALT5	ALT6	HDMI_CEC_IN
PAD329	KEY_COL3	U5	GPIO	ALT5	ALT4	I2C2_SCL
PAD330	KEY_ROW3	T7	GPIO	ALT5	ALT4	I2C2_SDA
PAD331	KEY_COL4	T6	GPIO	ALT5	ALT5	PCIE_DIS_B
PAD332	KEY_ROW4	V5	GPIO	ALT5	ALT5	N/A
PAD334	GPIO_0	T5	GPIO	ALT5	ALT0	GPIO_0_CLKO
PAD335	GPIO_1	T4	GPIO	ALT5	ALT4	SPKR
PAD336	GPIO_9	T2	GPIO	ALT5	ALT1	MX6_WDOG#
PAD337	GPIO_3	R7	GPIO	ALT5	ALT2	I2C3_SCL
PAD338	GPIO_6	T3	GPIO	ALT5	ALT2	I2C3_SDA
PAD340	GPIO_2	T1	GPIO	ALT5	ALT5	CSI1_ENA#
PAD341	GPIO_4	R6	GPIO	ALT5	ALT5	SYS_STATUS#
PAD342	GPIO_5	R4	GPIO	ALT5	ALT5	CSI1_RST#
PAD343	GPIO_7	R3	GPIO	ALT5	ALT3	CAN1_TX
PAD344	GPIO_8	R5	GPIO	ALT5	ALT3	CAN1_RX
PAD346	GPIO_16	R2	GPIO	ALT5	ALT5	N/A
PAD347	GPIO_17	R1	GPIO	ALT5	ALT5	PCIE_RST#
PAD348	GPIO_18	P6	GPIO	ALT5	ALT5	nSUSPEND
PAD349	GPIO_19	P5	GPIO	ALT5	ALT5	SLEEP_BTN#
PAD351	CSI0_PIXCLK	P1	IPU_CSI	ALT5	ALT5	N/A
PAD353	CSI0_MCLK	P4	IPU_CSI	ALT5	ALT3	CSI1_MCLK
PAD354	CSI0_DATA_EN	P3	IPU_CSI	ALT5	ALT5	N/A
PAD355	CSI0_VSYNC	N2	IPU_CSI	ALT5	ALT5	N/A
PAD356	CSI0_DAT4	N1	IPU_CSI	ALT5	ALT4	AUD3_TXC
PAD357	CSI0_DAT5	P2	IPU_CSI	ALT5	ALT4	AUD3_TXD
PAD359	CSI0_DAT6	N4	IPU_CSI	ALT5	ALT4	AUD3_TXFS
PAD360	CSI0_DAT7	N3	IPU_CSI	ALT5	ALT4	AUD3_RXD
PAD361	CSI0_DAT8	N6	IPU_CSI	ALT5	ALT4	I2C1_SDA
PAD362	CSI0_DAT9	N5	IPU_CSI	ALT5	ALT4	I2C1_SCL
PAD363	CSI0_DAT10	M1	IPU_CSI	ALT5	ALT3	UART1_TX
PAD365	CSI0_DAT11	M3	IPU_CSI	ALT5	ALT3	UART1_RX
PAD366	CSI0_DAT12	M2	IPU_CSI	ALT5	ALT3	UART4_TX
PAD367	CSI0_DAT13	L1	IPU_CSI	ALT5	ALT3	UART4_RX
PAD368	CSI0_DAT14	M4	IPU_CSI	ALT5	ALT5	N/A
PAD369	CSI0_DAT15	M5	IPU_CSI	ALT5	ALT5	N/A
PAD371	CSI0_DAT16	L4	IPU_CSI	ALT5	ALT3	UART4_RTS
PAD372	CSI0_DAT17	L3	IPU_CSI	ALT5	ALT3	UART4_CTS
PAD373	CSI0_DAT18	M6	IPU_CSI	ALT5	ALT5	N/A
PAD374	CSI0_DAT19	L6	IPU_CSI	ALT5	ALT5	CSI1_GPIO
PAD376	JTAG_TMS	C3	JTAG	ALT0	ALT0	JTAG_TMS
PAD378	JTAG_MOD	H6	JTAG	ALT0	ALT0	JTAG_MOD
PAD379	JTAG_TRSTB	C2	JTAG	ALT0	ALT0	JTAG_nTRST
PAD380	JTAG_TDI	G5	JTAG	ALT0	ALT0	JTAG_TDI
PAD381	JTAG_TCK	H5	JTAG	ALT0	ALT0	JTAG_TCK
PAD382	JTAG_TDO	G6	JTAG	ALT0	ALT0	JTAG_TDO
PAD385	LVDS1_TX3_P	AA4	LVDS	ALT0	ALT0	LVDS1_TX3_P
PAD386	LVDS1_TX3_N	AA3	LVDS			LVDS1_TX3_N
PAD387	LVDS1_TX2_P	AB2	LVDS	ALT0	ALT0	LVDS1_TX2_P
PAD388	LVDS1_TX2_N	AB1	LVDS			LVDS1_TX2_N
PAD391	LVDS1_CLK_P	Y4	LVDS	ALT0	ALT0	LVDS1_CLK_P
PAD392	LVDS1_CLK_N	Y3	LVDS			LVDS1_CLK_N
PAD393	LVDS1_TX1_P	AA1	LVDS	ALT0	ALT0	LVDS1_TX1_P
PAD394	LVDS1_TX1_N	AA2	LVDS			LVDS1_TX1_N
PAD397	LVDS1_TX0_P	Y2	LVDS	ALT0	ALT0	LVDS1_TX0_P
PAD398	LVDS1_TX0_N	Y1	LVDS			LVDS1_TX0_N
PAD399	LVDS0_TX3_P	W1	LVDS	ALT0	ALT0	LVDS0_TX3_P
PAD400	LVDS0_TX3_N	W2	LVDS			LVDS0_TX3_N
PAD403	LVDS0_CLK_P	V3	LVDS	ALT0	ALT0	LVDS0_CLK_P
PAD404	LVDS0_CLK_N	V4	LVDS			LVDS0_CLK_N
PAD405	LVDS0_TX2_P	V1	LVDS	ALT0	ALT0	LVDS0_TX2_P
PAD406	LVDS0_TX2_N	V2	LVDS			LVDS0_TX2_N
PAD409	LVDS0_TX1_P	U3	LVDS	ALT0	ALT0	LVDS0_TX1_P
PAD410	LVDS0_TX1_N	U4	LVDS			LVDS0_TX1_N
PAD411	LVDS0_TX0_P	U1	LVDS	ALT0	ALT0	LVDS0_TX0_P
PAD412	LVDS0_TX0_N	U2	LVDS			LVDS0_TX0_N
PAD415	PCIe_RXM	B1	PCIE			PCIE_RXM
PAD416	PCIe_TXP	B3	PCIE			PCIE_TXP
PAD417	PCIe_RXP	B2	PCIE			PCIE_RXP
PAD420	PCIe_TXM	A3	PCIE			PCIE_TXM
PAD431	CSI_D3P	F1	MIPI			CSI1_D3+
PAD432	CSI_D3M	F2	MIPI			CSI1_D3-
PAD433	CSI_D1P	D2	MIPI			CSI1_D1+
PAD436	CSI_D1M	D1	MIPI			CSI1_D1-
PAD437	CSI_CLK0P	F3	MIPI			CSI1_CLK0+
PAD438	CSI_CLK0M	F4	MIPI			CSI1_CLK0-
PAD441	CSI_D0P	E3	MIPI			CSI1_D0+
PAD442	CSI_D0M	E4	MIPI			CSI1_D0-
PAD443	CSI_D2P	E2	MIPI			CSI1_D2+
PAD446	CSI_D2M	E1	MIPI			CSI1_D2-
PAD447	DSI_D1P	H1	MIPI			N/A
PAD448	DSI_D1M	H2	MIPI			N/A
PAD451	DSI_REXT	G4	MIPI			N/A
PAD453	DSI_CLK0P	H4	MIPI			N/A
PAD454	DSI_CLK0M	H3	MIPI			N/A
PAD455	DSI_D0P	G1	MIPI			N/A
PAD458	DSI_D0M	G2	MIPI			N/A
PAD462	HDMI_D0P	K6	HDMI			HDMI_D0P
PAD463	HDMI_D0M	K5	HDMI			HDMI_D0M
PAD464	HDMI_D1P	J4	HDMI			HDMI_D1P
PAD466	HDMI_D1M	J3	HDMI			HDMI_D1M
PAD467	HDMI_D2P	K4	HDMI			HDMI_D2P
PAD468	HDMI_D2M	K3	HDMI			HDMI_D2M
PAD469	HDMI_CLKP	J6	HDMI			HDMI_CLKP
PAD470	HDMI_CLKM	J5	HDMI			HDMI_CLKM
PAD473	HDMI_HPD	K1	HDMI			HDMI_HPD
PAD476	USB_H1_DP	E10	ANATOP			USB_HOST_DP
PAD477	USB_H1_DN	F10	ANATOP			USB_HOST_DN
PAD482	USB_OTG_CHD_B	B8	ANATOP			N/A
PAD483	USB_OTG_DN	B6	ANATOP			USB_OTG_DN
PAD484	USB_OTG_DP	A6	ANATOP			USB_OTG_DP
PAD495	CLK1_P	D7	ANATOP			PCIe_C_CREFCLKP
PAD496	CLK1_N	C7	ANATOP			PCIe_C_CREFCLKM
PAD497	CLK2_P	D5	ANATOP			N/A
PAD498	CLK2_N	C5	ANATOP			N/A
PAD512	SATA_TXM	B12	SATA			SATA_C_TXN
PAD513	SATA_TXP	A12	SATA			SATA_C_TXP
PAD514	SATA_RXP	B14	SATA			SATA_C_RXP
PAD515	SATA_RXM	A14	SATA			SATA_C_RXN
PAD520	TAMPER	E11	RESET	ALT0	ALT0	TAMPER
PAD522	PMIC_ON_REQ	D11	RESET	ALT0	ALT0	PMIC_ON_REQ
PAD523	PMIC_STBY_REQ	F11	RESET	ALT0	ALT0	PMIC_STBY_REQ
PAD524	POR_B	C11	RESET	ALT0	ALT0	POR#
PAD525	BOOT_MODE1	F12	RESET	ALT0	ALT0	BOOT_MODE1
PAD526	RESET_IN_B	D12	RESET	ALT0	ALT0	SOC_ONOFF
PAD529	BOOT_MODE0	C12	RESET	ALT0	ALT0	BOOT_MODE0
PAD530	TEST_MODE	E12	RESET	ALT0	ALT0	TEST_MODE
PAD543	SD3_DAT7	F13	SD_3	ALT5	ALT0	SD3_Q7_DATA7
PAD544	SD3_DAT6	E13	SD_3	ALT5	ALT0	SD3_Q7_DATA6
PAD545	SD3_DAT5	C13	SD_3	ALT5	ALT0	SD3_Q7_DATA5
PAD546	SD3_DAT4	D13	SD_3	ALT5	ALT0	SD3_Q7_DATA4
PAD549	SD3_CMD	B13	SD_3	ALT5	ALT0	SD3_Q7_CMD
PAD550	SD3_CLK	D14	SD_3	ALT5	ALT0	SD3_Q7_CLK
PAD551	SD3_DAT0	E14	SD_3	ALT5	ALT0	SD3_Q7_DATA0
PAD552	SD3_DAT1	F14	SD_3	ALT5	ALT0	SD3_Q7_DATA1
PAD555	SD3_DAT2	A15	SD_3	ALT5	ALT0	SD3_Q7_DATA2
PAD556	SD3_DAT3	B15	SD_3	ALT5	ALT0	SD3_Q7_DATA3
PAD557	SD3_RST	D15	SD_3	ALT5	ALT5	SD3_Q7_ACT#
PAD559	NANDF_CE	C15	NANDF	ALT5	ALT5	LVDS_PPEN
PAD562	NANDF_ALE	A16	NANDF	ALT5	ALT5	WDTRIG#
PAD563	NANDF_WP_B	E15	NANDF	ALT5	ALT5	LVDS_BLEN
PAD564	NANDF_RB0	B16	NANDF	ALT5	ALT5	WDT_EN
PAD565	NANDF_CS0	F15	NANDF	ALT5	ALT5	GPIO_Q7-1
PAD568	NANDF_CS1	C16	NANDF	ALT5	ALT5	GPIO_Q7-2
PAD569	NANDF_CS2	A17	NANDF	ALT5	ALT5	GPIO_Q7-3
PAD570	NANDF_CS3	D16	NANDF	ALT5	ALT5	GPIO_Q7-4
PAD571	SD4_CMD	B17	NANDF	ALT5	ALT0	SD4_MMC_CMD
PAD574	SD4_CLK	E16	NANDF	ALT5	ALT0	SD4_MMC_CLK
PAD575	NANDF_D0	A18	NANDF	ALT5	ALT5	SD2_MICRO_CD#
PAD576	NANDF_D1	C17	NANDF	ALT5	ALT5	SD3_Q7_CD#
PAD577	NANDF_D2	F16	NANDF	ALT5	ALT5	SD3_Q7_PWREN#
PAD580	NANDF_D3	D17	NANDF	ALT5	ALT5	SD3_Q7_WP
PAD581	NANDF_D4	A19	NANDF	ALT5	ALT5	N/A
PAD582	NANDF_D5	B18	NANDF	ALT5	ALT5	N/A
PAD583	NANDF_D6	E17	NANDF	ALT5	ALT5	N/A
PAD586	NANDF_D7	C18	NANDF	ALT5	ALT5	N/A
PAD587	SD4_DAT0	D18	NANDF	ALT5	ALT1	SD4_MMC_DATA0
PAD588	SD4_DAT1	B19	NANDF	ALT5	ALT1	SD4_MMC_DATA1
PAD589	SD4_DAT2	F17	NANDF	ALT5	ALT1	SD4_MMC_DATA2
PAD592	SD4_DAT3	A20	NANDF	ALT5	ALT1	SD4_MMC_DATA3
PAD593	SD4_DAT4	E18	NANDF	ALT5	ALT1	SD4_MMC_DATA4
PAD594	SD4_DAT5	C19	NANDF	ALT5	ALT1	SD4_MMC_DATA5
PAD595	SD4_DAT6	B20	NANDF	ALT5	ALT1	SD4_MMC_DATA6
PAD598	SD4_DAT7	D19	NANDF	ALT5	ALT1	SD4_MMC_DATA7
PAD600	SD1_DAT1	C20	SD1	ALT5	ALT5	SPI5_CS0#
PAD601	SD1_DAT0	A21	SD1	ALT5	ALT1	SPI5_MISO
PAD602	SD1_DAT3	F18	SD1	ALT5	ALT5	LVDS_CONTRAST
PAD605	SD1_CMD	B21	SD1	ALT5	ALT1	SPI5_MOSI
PAD606	SD1_DAT2	E19	SD1	ALT5	ALT5	SPI5_CS1#
PAD607	SD1_CLK	D20	SD1	ALT5	ALT1	SPI5_SCLK
PAD610	SD2_CLK	C21	SD2	ALT5	ALT0	SD2_MICRO_CLK
PAD611	SD2_CMD	F19	SD2	ALT5	ALT0	SD2_MICRO_CMD
PAD612	SD2_DAT3	B22	SD2	ALT5	ALT0	SD2_MICRO_DATA3

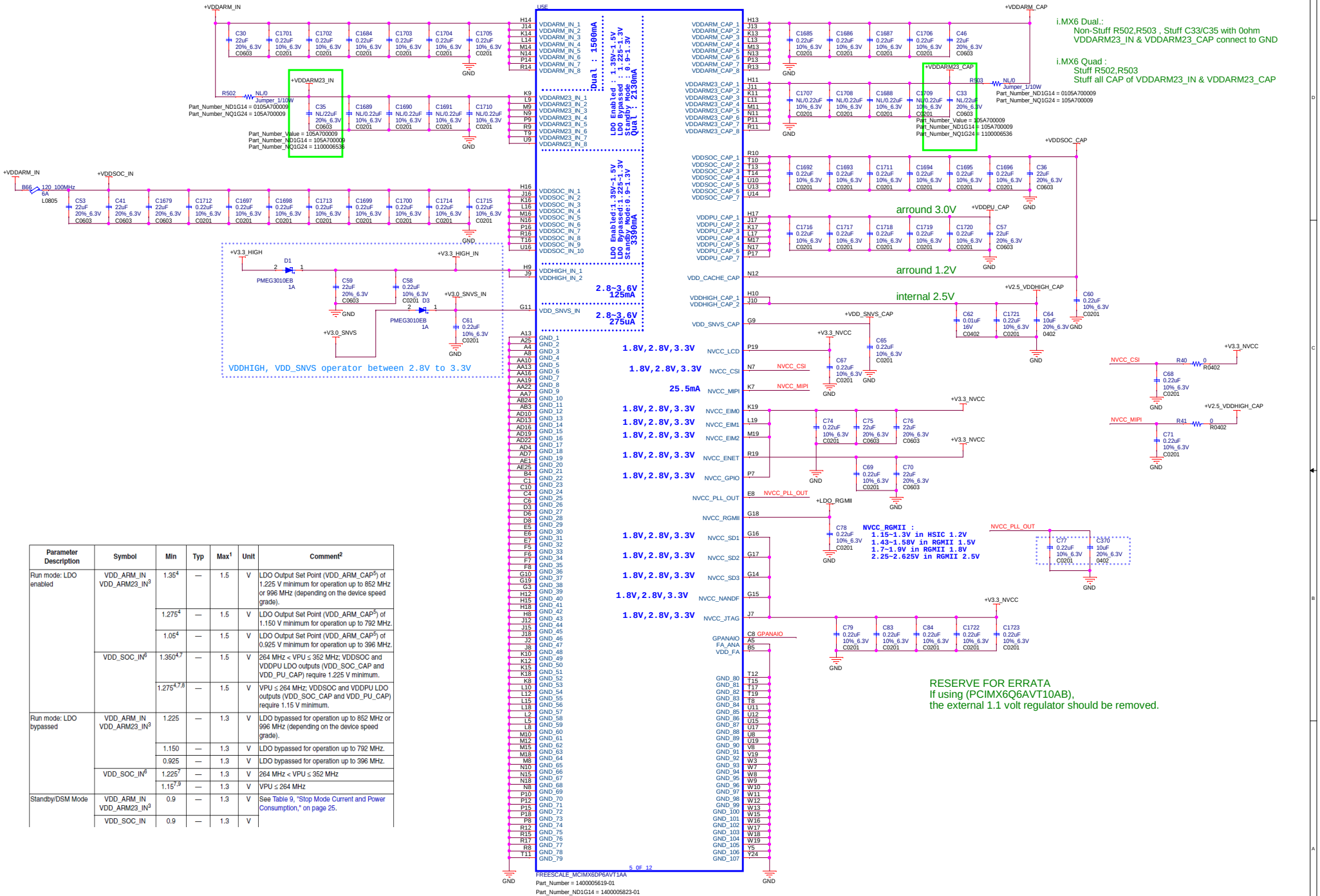
ADVANTECH

Title: PIN MUX TABLE

Size | Document Number: ROM-7421 | Rev: 1000-3

Date: Monday, September 24, 2018 | Sheet 5 of 18

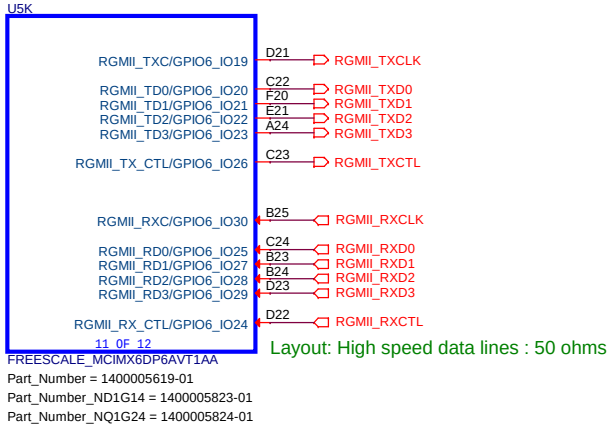

TPS65911
141_TI_TPS659114_0
Part_Number = 1410026452-01
Manufacture_Part_Number = TPS659114A2ZRCR
CLOCK
REFERENCE
GPIO
CONTROL
TEST
DCDC CTRL
SMPS
VDD1
VDD2
VIO
GND
AUTO BTN
A101-2.3
A101-3.3
A101-3.4
A101-3.2
A101-2.11
Vout = 0.8*(1+(56.2K/17.4K)) = 3.38V
ADVANTECH
POWER_PMIC(TPS65911)
ROM-7421
Monday, September 26, 2016



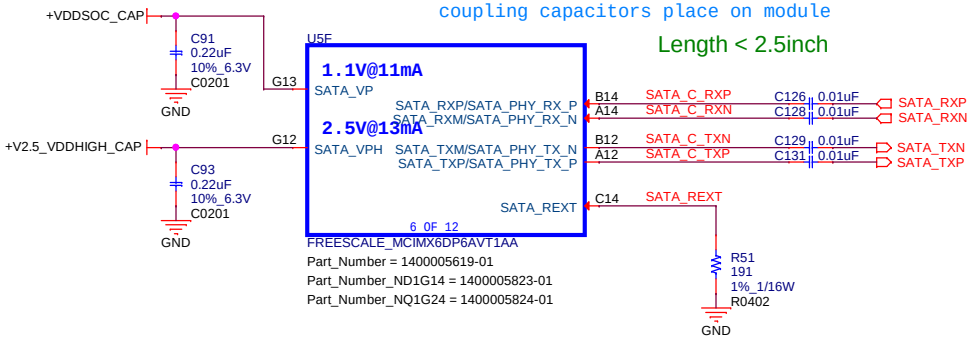
Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN VDD_ARM23_IN[3]	1.35[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.225 V minimum for operation up to 852 MHz or 996 MHz (depending on the device speed grade).
		1.275[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 1.150 V minimum for operation up to 792 MHz.
		1.05[4]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP[5]) of 0.925 V minimum for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.350[4,7]	—	1.5	V	264 MHz < VPU ≤ 352 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.225 V minimum.
		1.275[4,7,8]	—	1.5	V	VPU ≤ 264 MHz; VDDSOC and VDDPU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN VDD_ARM23_IN[3]	1.225	—	1.3	V	LDO bypassed for operation up to 852 MHz or 996 MHz (depending on the device speed grade).
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz.
		0.925	—	1.3	V	LDO bypassed for operation up to 396 MHz.
	VDD_SOC_IN[6]	1.225[7]	—	1.3	V	264 MHz < VPU ≤ 352 MHz
		1.15[7,9]	—	1.3	V	VPU ≤ 264 MHz
Standby/DSM Mode	VDD_ARM_IN VDD_ARM23_IN[3]	0.9	—	1.3	V	See Table 9, "Stop Mode Current and Power Consumption," on page 25.
	VDD_SOC_IN	0.9	—	1.3	V	

ADVANTECH

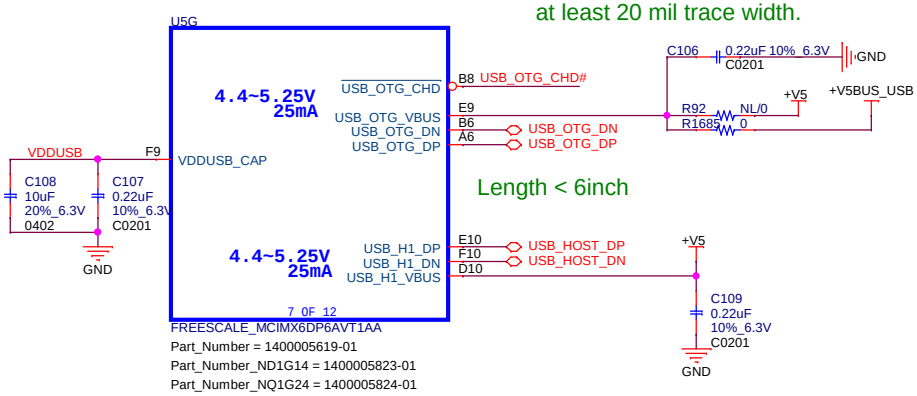
Title	CPU POWER	
Size	Document Number ROM-7421	Rev A101-3
Date: Monday, September 26, 2016	Sheet 7 of 18	

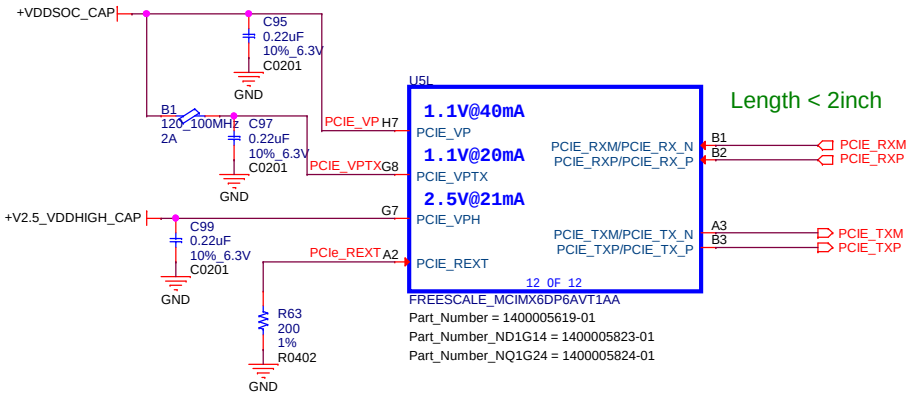


Layout: High speed data lines : 50 ohms



at least 20 mil trace width.





ADVANTECH

Title	MX6_I/O1_RGMII_SATA_USB_PCIe	
Size	Document Number ROM-7421	Rev A101-3
Date: Monday, September 26, 2016	Sheet 8 of 18	

SD/eMMC/LCD : The Group Length matching should within +/-40mil (total)

add net: USB_HOST_PRES#

USB_OTG_ID don't need to pull up. follow freescale CRB

Close MXM Connector

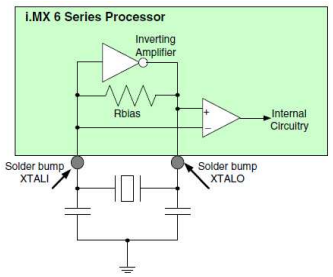
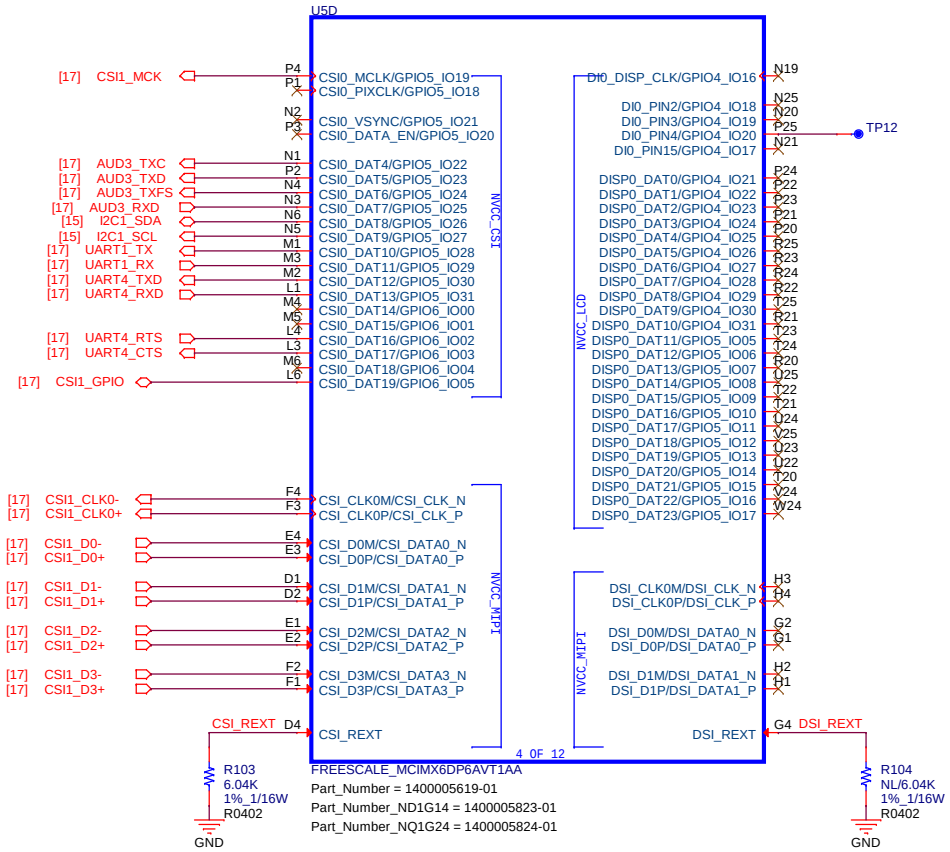
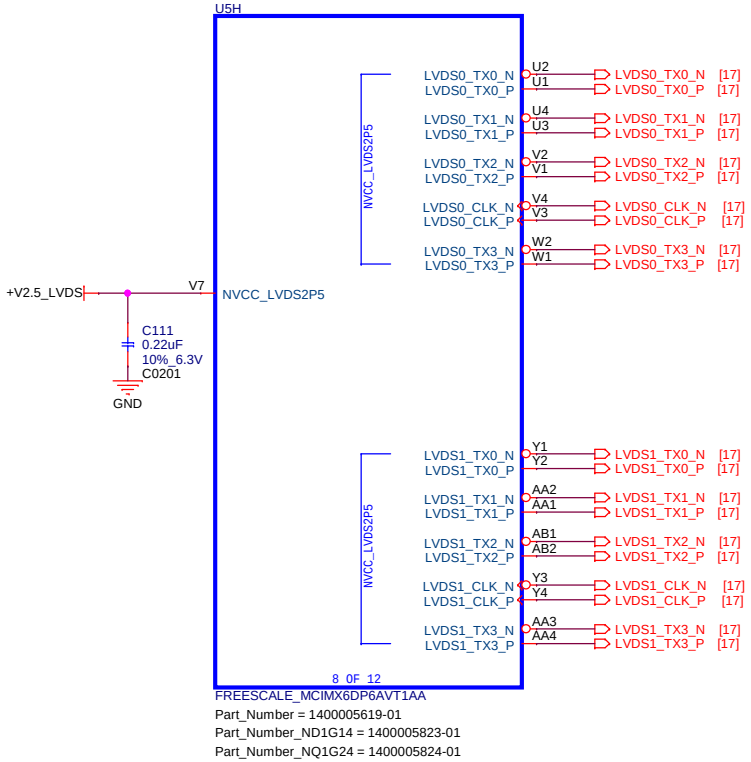
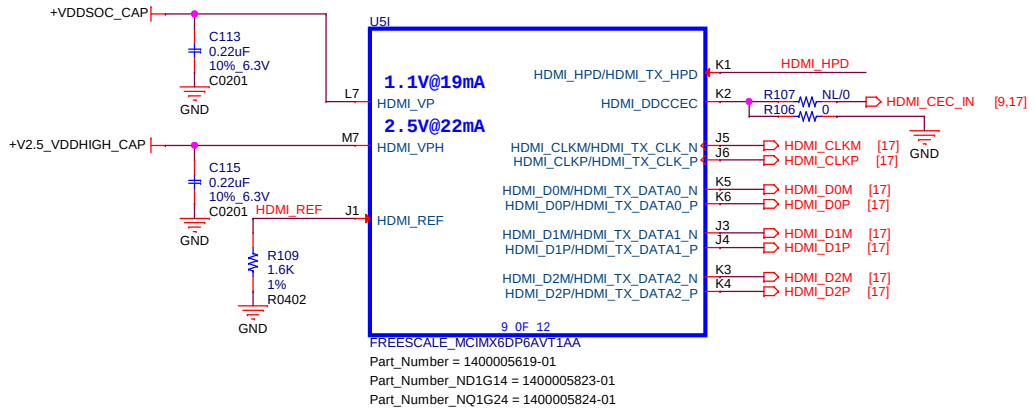


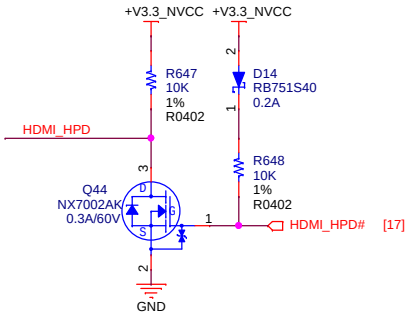
Figure 69-1. Oscillator Configuration (24 MHz)

Title	MX6_I/O2_EIM_CTRL_GPIO_SDIO
Size	Document Number ROM-7421 Rev A101-3
Date:	Monday, September 26, 2016 Sheet 9 of 18





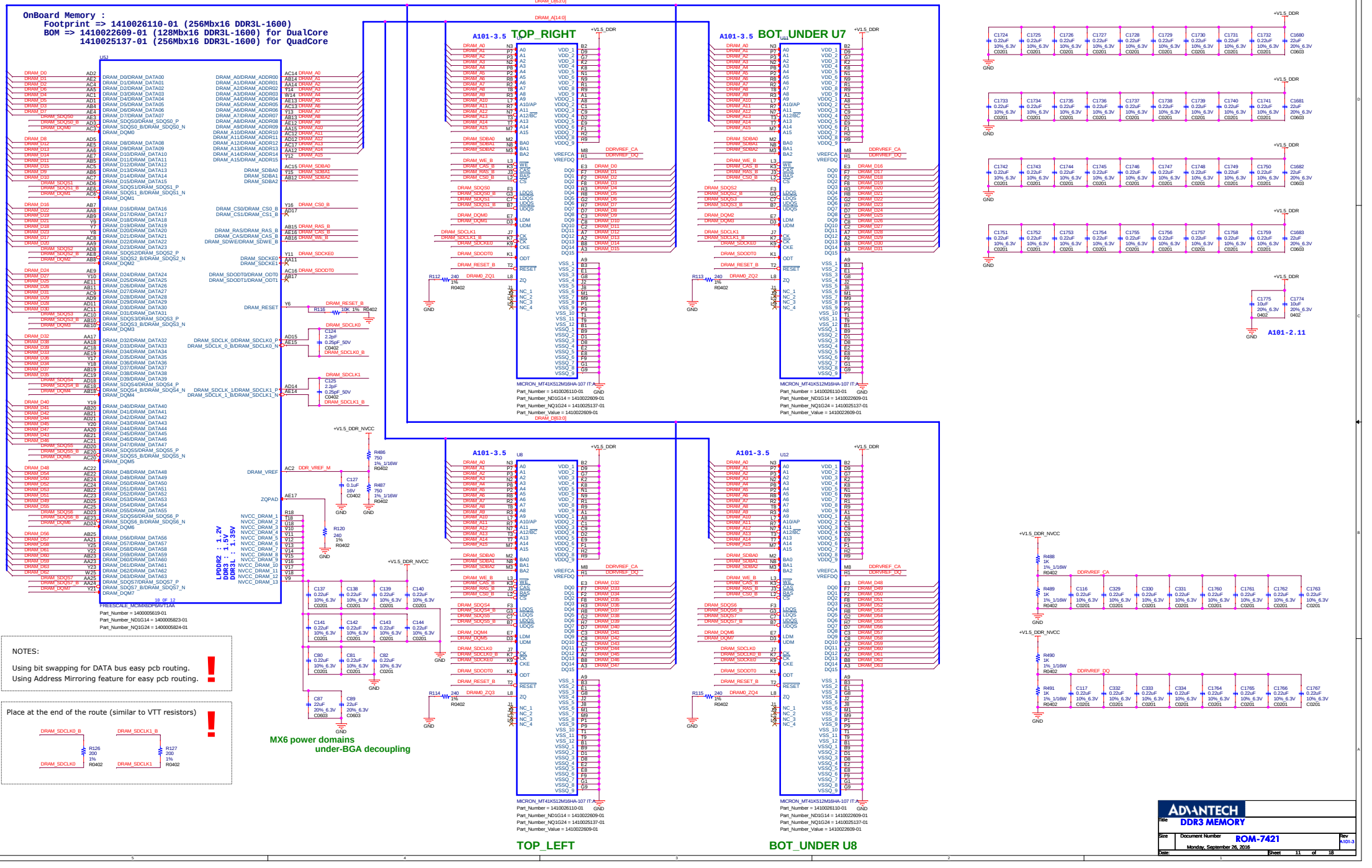




ADVANTECH

Title	MX6_I/O3_DISP.CSI_LVDS_HDMI	
Size	Document Number ROM-7421	Rev A101-3
Date: Monday, September 26, 2016	Sheet 10 of 18	

OnBoard Memory :
Footprint => 1410026110-01 (256Mbx16 DDR3L-1600)
BOM => 1410022609-01 (128Mbx16 DDR3L-1600) for DualCore
1410025137-01 (256Mbx16 DDR3L-1600) for QuadCore



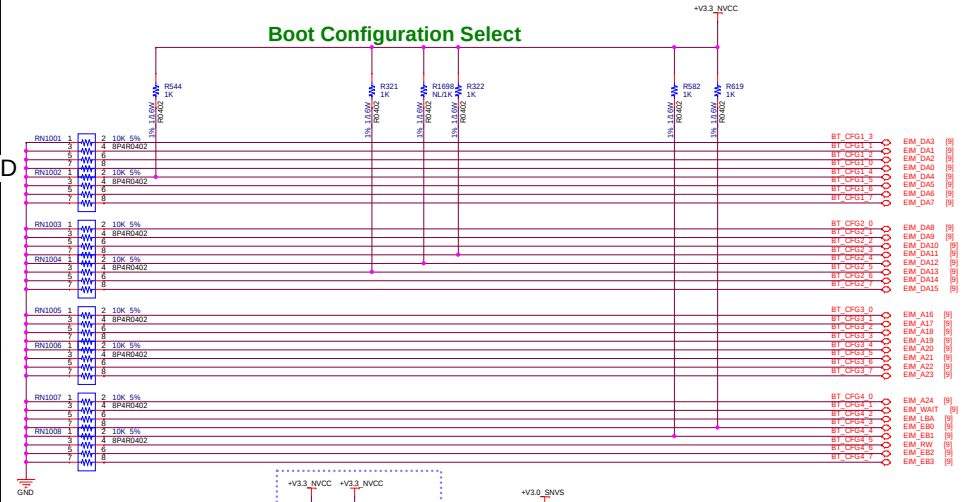
NOTES:

Using bit swapping for DATA bus easy pcb routing.
Using Address Mirroring feature for easy pcb routing.

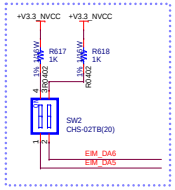
Place at the end of the route (similar to VTT resistors)

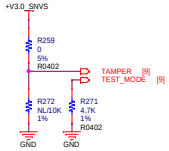
Title	DDR3 MEMORY
Size	Document Number ROM-7421 Rev A101-3
Date:	Monday, September 26, 2016 Sheet 11 of 18

Boot Configuration Select



	EIM_DA5	EIM_DA6
Serial-ROM SPI1 CS1	1	0
SD/eSD SD2	0	1



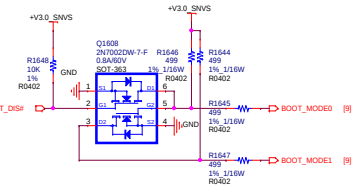


Boot from external SD or internal SPI NOR

Boot Mode

BOOT_MODE[1]	BOOT_MODE[0]	Boot Type	Boot Details
0	0	Boot from fuses	Like 10, but boot fuses will be always used, if BT_FUSE_SEL=1
0	1	Serial Download via USB	Load and execute code, via serial device: USB (high-speed, non-stream, bulk mode)
1	**0**	**Normal Boot (Development)**	**Executing ROM code, which handles booting from following sources** **NOR Flash (via WEIM, 16-bit, slow asynchronous mode for debugging purpose only)** **OneNAND** **SPI (serial flash) / I2C** **NAND Flash** **SD/MMC /MoviNAND** **SATA (Hard disk or SSD)** **A fallback to ALL above modes, on error exception: USB** **If BT_FUSE_SEL=0, GPIO boot pins will be sampled.**
1	1	FSL Test Mode	Freescale Test Mode, special mode reserved for device testing.

BOOT MODES[1:0]:
00 Boot from fuses
01 Serial downloader---MFG TOOL
10 Boot from board settings
11 Reserved



Reserved configuration switch should be set to '0' (OFF)

SW4

	BOOT_CFG4 [7]	BOOT_CFG4 [6]	BOOT_CFG4 [5]	BOOT_CFG4 [4]	BOOT_CFG4 [3]	BOOT_CFG4 [2]	BOOT_CFG3 [1]	BOOT_CFG3 [0]
	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)		Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - eCSPI5 101 - I2C1 110 - I2C2 111 - I2C3	

Reserved configuration switch should be set to '0' (OFF)

SW1

	BOOT_CFG1 [7]	BOOT_CFG1 [6]	BOOT_CFG1 [5]	BOOT_CFG1 [4]	BOOT_CFG1 [3]	BOOT_CFG1 [2]	BOOT_CFG1 [1]	BOOT_CFG1 [0]
Reserved-NVM	0	0	0	1	Reserved	Reserved	Reserved	Reserved
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
SATA	0	0	1	0	Reserved	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		Reserved (SDXC power control - XPC) 100mA/150mA TBD	SD Loopback Clock Source Sel '0' - direct '1' - through SD pad
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - Highl 1- Normal	Reserved	Reserved	MMC Loopback Clock Source Sel '0' - direct '1' - through SD pad
NAND	1	Reserved (Freq select)	BT_TOGGLEMODE	Override Pad Settings (using PAD_SETTINGS value)	Interleave Scheme: (TBD)		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

Reserved configuration switch should be set to '0' (OFF)

SW2

	BOOT_CFG2 [7]	BOOT_CFG2 [6]	BOOT_CFG2 [5]	BOOT_CFG2 [4]	BOOT_CFG2 [3]	BOOT_CFG2 [2]	BOOT_CFG2 [1]	BOOT_CFG2 [0]
Reserved-NVM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
WEIM	Muxing Scheme: A/D16 (HW Default in external boot) A+DH ,A+DL A/D32		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Reserved	Reserved	Reserved
SATA	Reserved	Reserved	Reserved	Tx Spread Spectrum '0' - Disabled '1' - Enabled	Rx Spread Spectrum '0' - Disabled '1' - Enabled	SATA_SPEED 0 - Gen2 (3.0Gbps) 1 - Gen1 (1.5Gbps)	SATA Type: '00' - I '01' - m '10' - x '11' - Reserved	
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3 11 - eSDHC4		Reserved (SDXC Current Limit) 200mA/400mA/600mA/800mA (TBD)		Override Pad Settings (using PAD_SETTINGS value)
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3 11 - eSDHC4		DLL Override: 0 - Boot ROM default. 1 - Apply value per fuse field MMC_DLL_DLY[3:0]	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	Override Pad Settings (using PAD_SETTINGS value)
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Pages In Block: 00 - 128 01 - 64 10 - 32 11 - Reserved		TBD (LBA-Nand) 0 - Non LBA (11ms delay) 1 - LBA (22ms delay)

Reserved configuration switch should be set to '0' (OFF)

SW3

	BOOT_CFG3 [7]	BOOT_CFG3 [6]	BOOT_CFG3 [5]	BOOT_CFG3 [4]	BOOT_CFG3 [3]	BOOT_CFG3 [2]	BOOT_CFG3 [1]	BOOT_CFG3 [0]
	L1 I-Cache DISABLE	BT_MMU_DISABLE	DDR Memory Map default config '00' - Single DDR channel '01' - Fixed 2x32 map '10' - 4KB Interleaving Enabled '11' - Illegal		Reserved (DDR3 SPI config) '1' - DDR3 config. Read via SPI.	Boot Frequencies (ARM/DDR) 0 - 792 / 528 MHz 1 - 528 / 352MHz	Reserved	Reserved

ADVANTECH

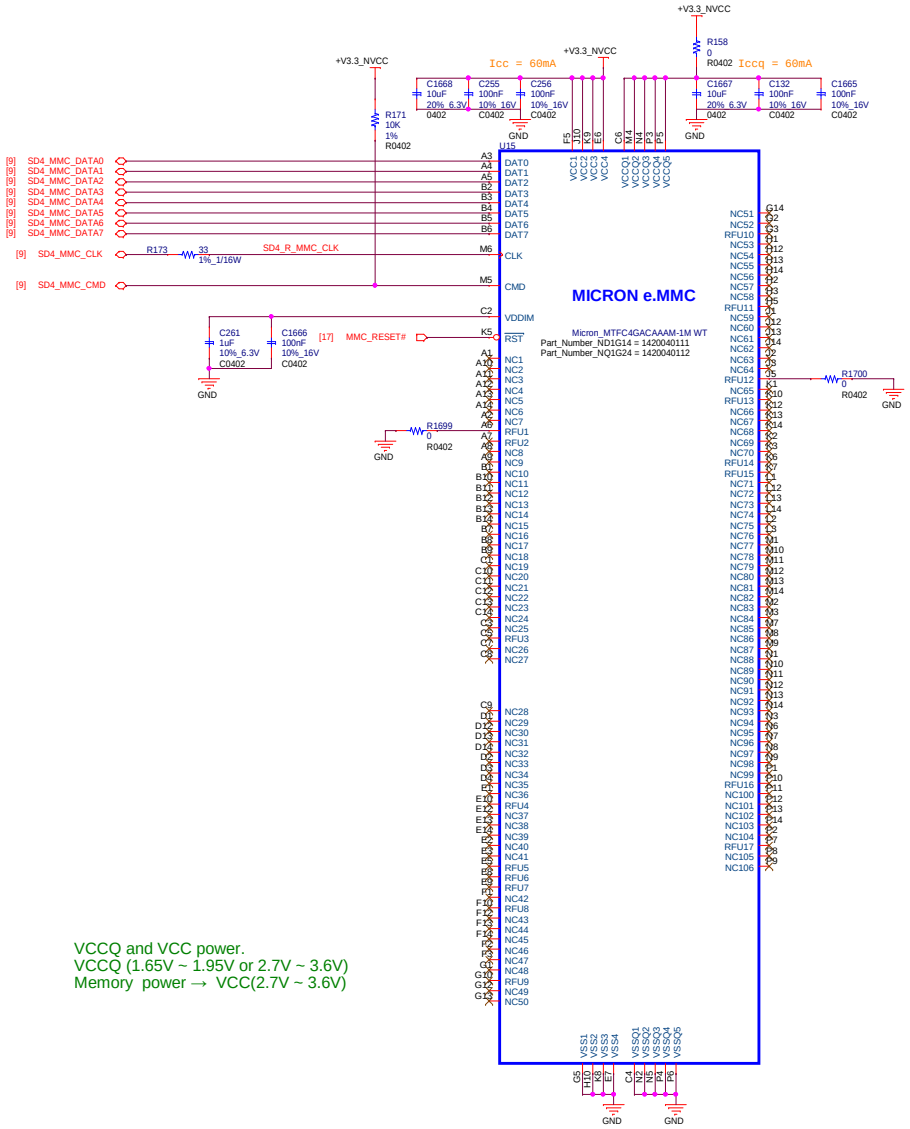
Title: BOOT SELECT

Size: | Document Number: ROM-7421 | Rev: A101-3

Date: Monday, September 26, 2016 | Sheet 12 of 18

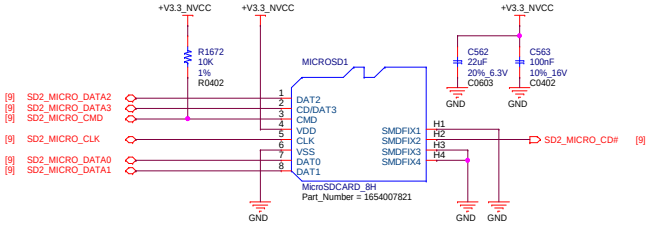
eMMC

Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

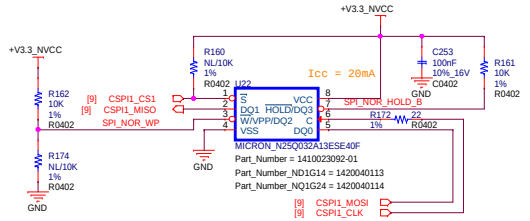


VCCQ and VCC power.
VCCQ (1.65V ~ 1.95V or 2.7V ~ 3.6V)
Memory power → VCC(2.7V ~ 3.6V)

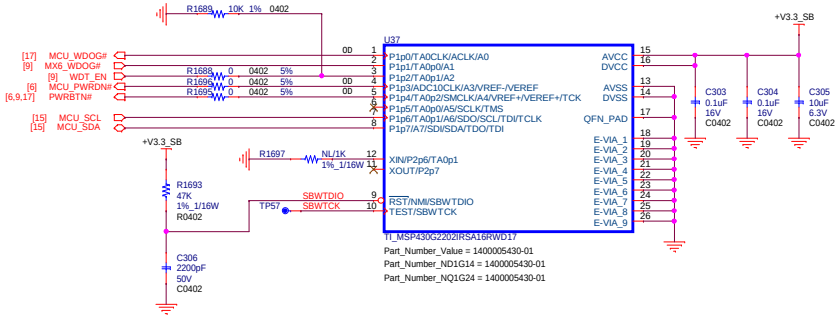
Micro SD



SPI NOR FLASH



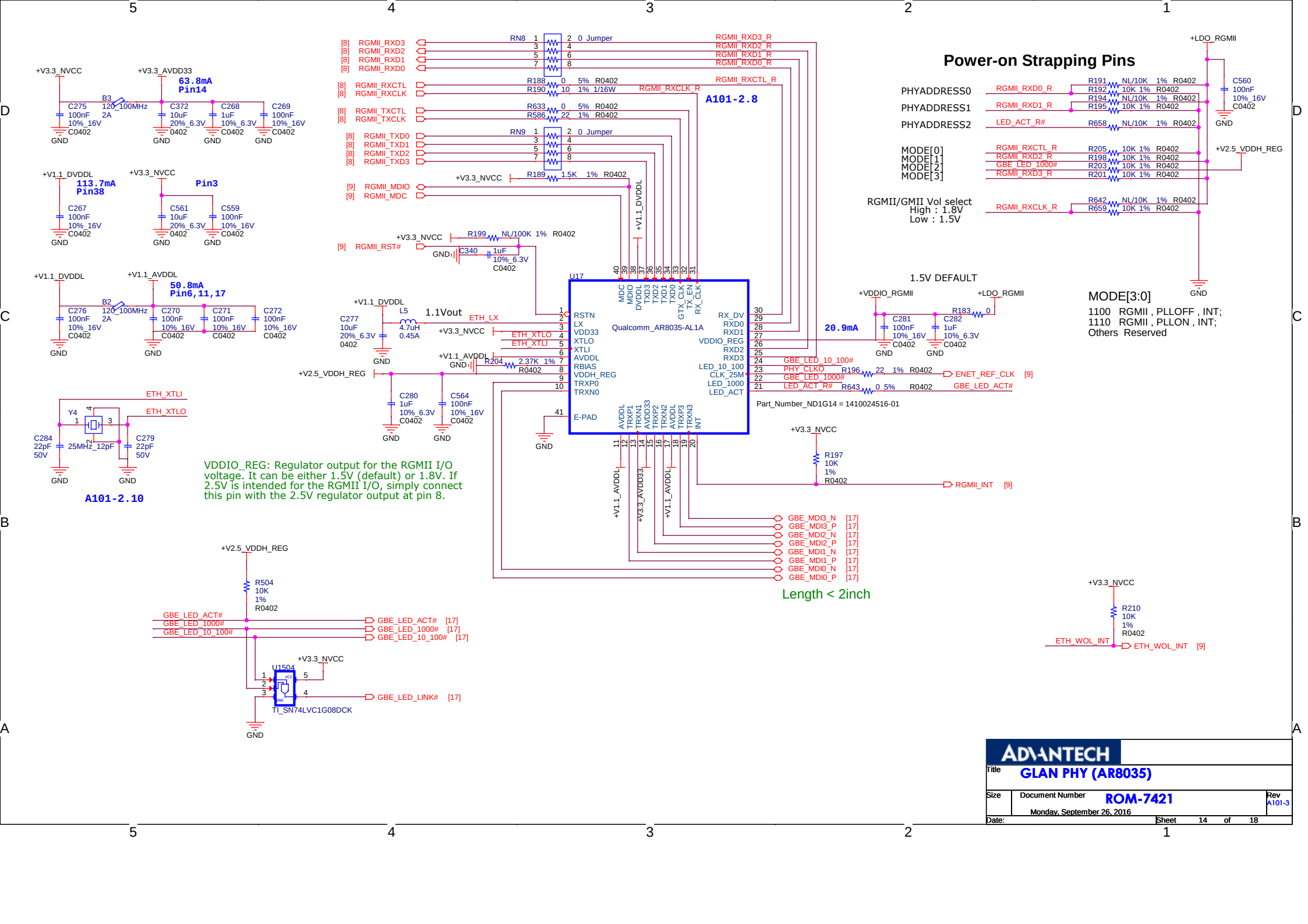
WDT



1. Reset path : Q7_CarryBrd => (WDTRIG#) => i.MX6 => (MX_WDOG#) => MCU
2. H/W WDT Reset circuit :
   - <1> Programming the WDT's parameter through MCU_SCL/SDA
   - <2> Enable WDT function by signal: WDT_EN
   - <3> If time out , then MCU will reset the system by signal : MCU_WDOG#
   - <4> If the system can't be reset by POR# , then MCU_PWRDN# will drive to low level (cause PMIC's shutdown event) first , and trigger the PWRBTN# event.

ADVANTECH

Title	eMMC_MicroSD_SPI FLASH_WDT	
Size	Document Number ROM-7421	Rev A101-3
Date: Monday, September 26, 2016	Sheet 13 of 18	


Power-on Strapping Pins
PHYADDRESS0
PHYADDRESS1
PHYADDRESS2
MODE[0]
MODE[1]
MODE[2]
MODE[3]
RGMII/GMII Vol select
High : 1.8V
Low : 1.5V
MODE[3:0]
1100 RGMII , PLLOFF , INT;
1110 RGMII , PLLON , INT;
Others Reserved
1.5V DEFAULT
Qualcomm_AR8035-AL1A
Part_Number_ND1G14 = 1410024516-01
A101-2.8
A101-2.10
VDDIO_REG: Regulator output for the RGMII I/O voltage. It can be either 1.5V (default) or 1.8V. If 2.5V is intended for the RGMII I/O, simply connect this pin with the 2.5V regulator output at pin 8.
Length < 2inch
TI_SN74LVC1G08DCK
ADVANTECH
Title
GLAN PHY (AR8035)
Size
Document Number
ROM-7421
Rev
A101-3
Date:
Monday, September 26, 2016
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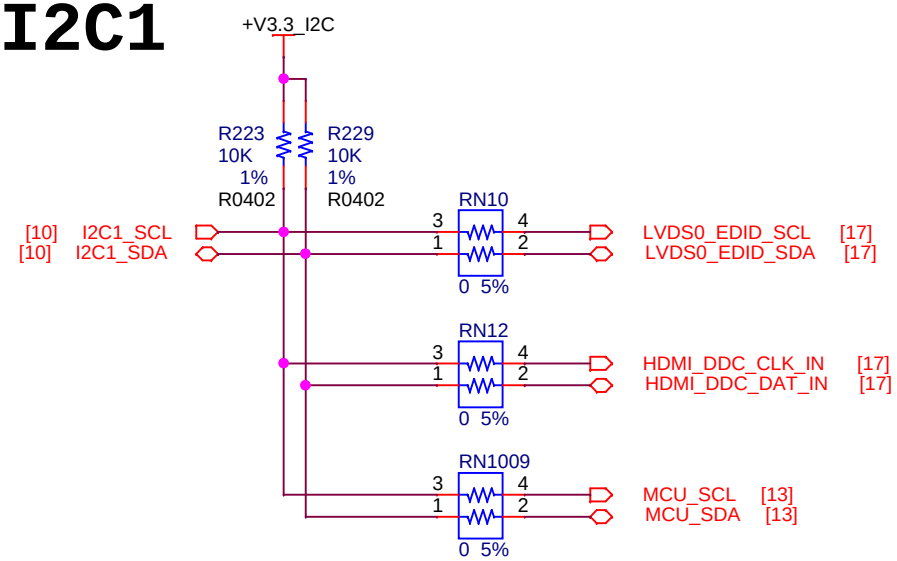
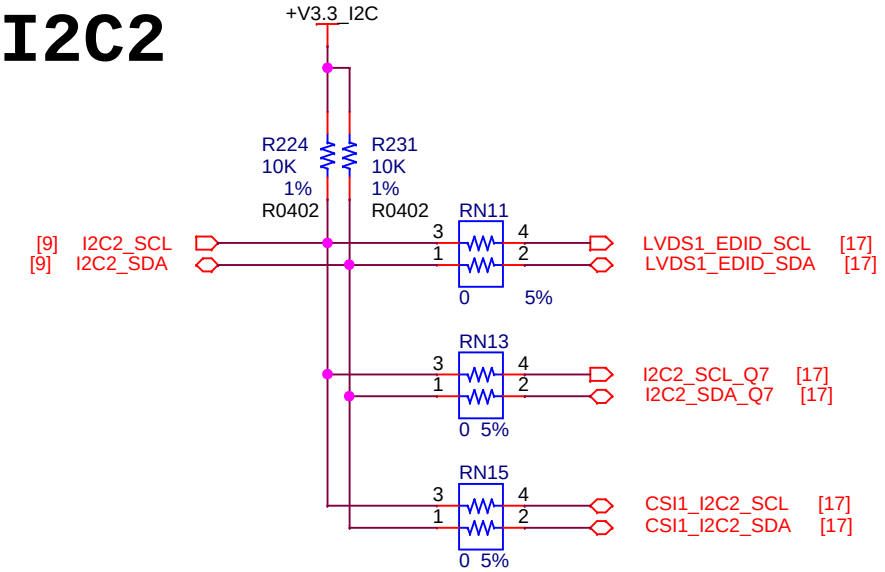
I2C1



I2C2

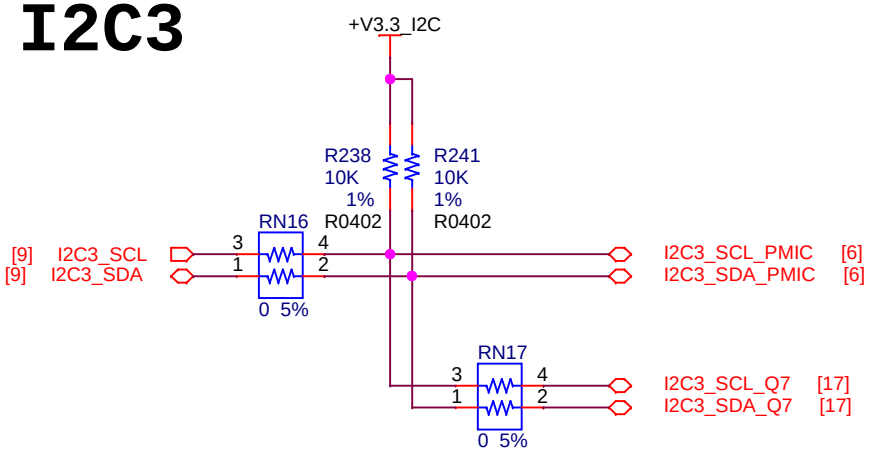


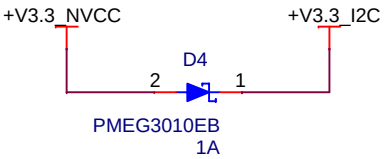
Channel - i2c0
- |-> LVDS0
- |-> HDMI (Addr.0x3a/0x50)
- |-> WDT_MCU (Addr.0x29)

Channel - i2c1
- |-> LVDS1
- |-> MIPI
- |-> i2c_switch(Addr.0x70)
  - |=> I2C_PinHeader
  - |=> CODEC_SGTL5000 (Addr.0x0a)

Channel - i2c2
- |-> PMIC (Addr.0x2d)
- |-> EC_IT8566E (Addr.0x30/0x66)

I2C3





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Title	I2C COMM CHANNEL	
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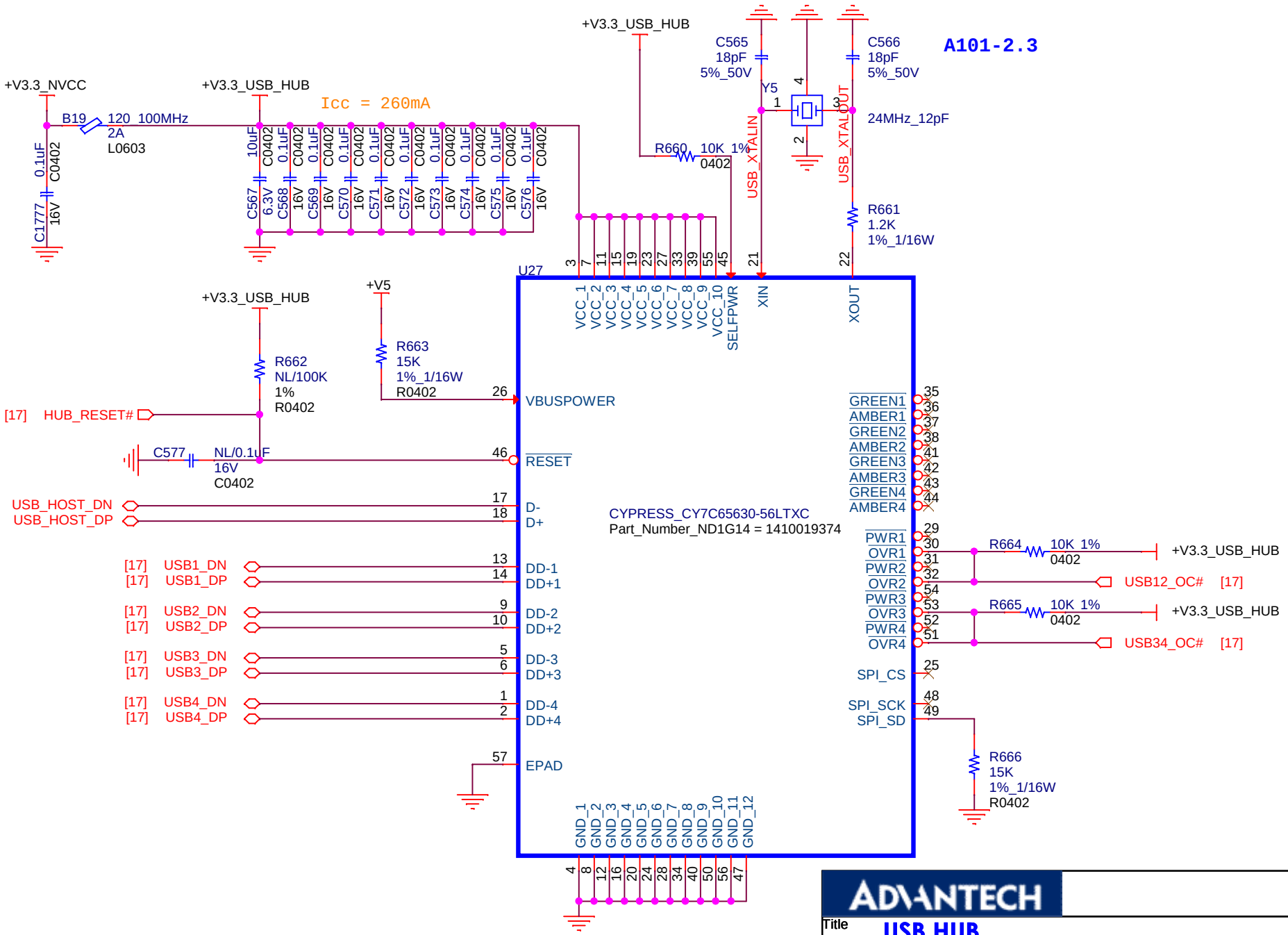
A101-2.3
+V3.3_NVCC
+V3.3_USB_HUB
Icc = 260mA
B19
120_100MHz
2A
L0603
0.1uF C0402
C1777 16V
10uF C0402
0.1uF C0402
C567 6.3V
C568 16V
C569 16V
C570 16V
C571 16V
C572 16V
C573 16V
C574 16V
C575 16V
C576 16V
+V3.3_USB_HUB
C565
18pF
5%_50V
C566
18pF
5%_50V
Y5
24MHz_12pF
USB_XTALIN
USB_XTALOUT
R660 10K 1%
0402
R661
1.2K
1%_1/16W
U27
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
SELFPWR
XIN
XOUT
+V3.3_USB_HUB
+V5
R662
NL/100K
1%
R0402
R663
15K
1%_1/16W
R0402
[17] HUB_RESET#
C577 NL/0.1uF
16V
C0402
VBUSPOWER
RESET
[8] USB_HOST_DN
[8] USB_HOST_DP
D-
D+
CYPRESS_CY7C65630-56LTXC
Part_Number_ND1G14 = 1410019374
[17] USB1_DN
[17] USB1_DP
DD-1
DD+1
[17] USB2_DN
[17] USB2_DP
DD-2
DD+2
[17] USB3_DN
[17] USB3_DP
DD-3
DD+3
[17] USB4_DN
[17] USB4_DP
DD-4
DD+4
EPAD
GREEN1
AMBER1
GREEN2
AMBER2
GREEN3
AMBER3
GREEN4
AMBER4
PWR1
OVR1
PWR2
OVR2
PWR3
OVR3
PWR4
OVR4
R664 10K 1%
0402
+V3.3_USB_HUB
USB12_OC# [17]
R665 10K 1%
0402
+V3.3_USB_HUB
USB34_OC# [17]
SPI_CS
SPI_SCK
SPI_SD
R666
15K
1%_1/16W
R0402
GND_1
GND_2
GND_3
GND_4
GND_5
GND_6
GND_7
GND_8
GND_9
GND_10
GND_11
GND_12
ADVANTECH
Title
USB HUB
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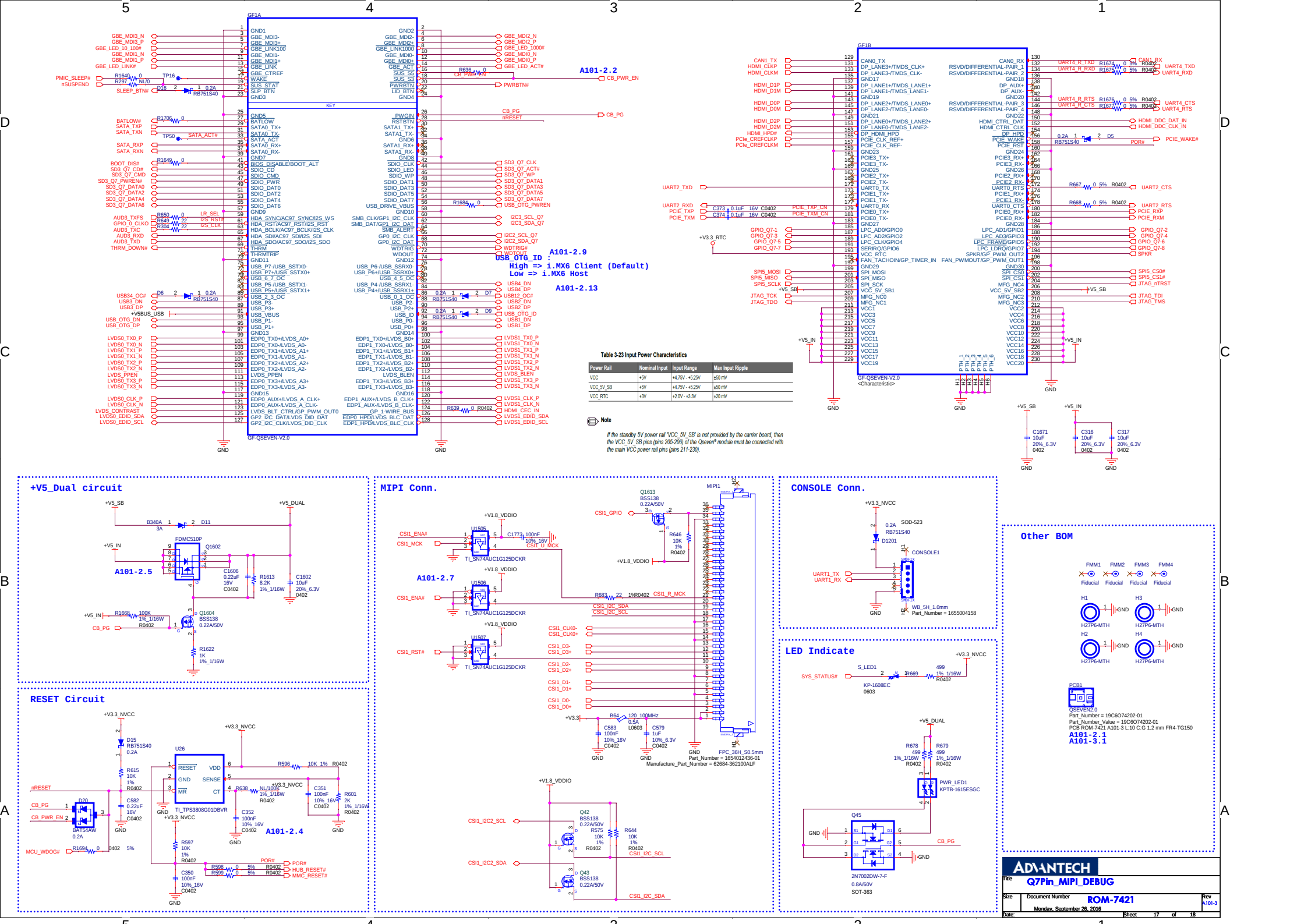
GF1A
GF1B
GF-QSEVEN-V2.0
A101-2.2
A101-2.9
USB_OTG_ID :
High => i.MX6 Client (Default)
Low => i.MX6 Host
A101-2.13
Table 3-23 Input Power Characteristics
Power Rail | Nominal Input | Input Range | Max Input Ripple
VCC | +5V | +4.75V - +5.25V | ±50 mV
VCC_5V_SB | +5V | +4.75V - +5.25V | ±50 mV
VCC_RTC | +3V | +2.0V - +3.3V | ±20 mV
Note
If the standby 5V power rail 'VCC_5V_SB' is not provided by the carrier board, then the VCC_5V_SB pins (pins 205-206) of the Qseven® module must be connected with the main VCC power rail pins (pins 211-230).
+V5_Dual circuit
A101-2.5
RESET Circuit
A101-2.4
MIPI Conn.
A101-2.7
CONSOLE Conn.
LED Indicate
Other BOM
FMM1 FMM2 FMM3 FMM4
Fiducial
H1 H2 H3 H4
H27P6-MTH
PCB1
QSEVEN2.0
Part_Number = 19C6O74202-01
Part_Number_Value = 19C6O74202-01
PCB ROM-7421 A101-3 L:10 C:G 1.2 mm FR4-TG150
A101-2.1
A101-3.1
ADVANTECH
Title
Q7Pin_MIPI_DEBUG
Size
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ROM-7421 A101-1 PCB:19C6O74200-01, 96 BOM:9696O74200E Date: 2015/09/24

1. First release.

ROM-7421 A101-2 PCB:19C6O74201-01, 96 BOM:9696O74200E Date: 2015/09/24

1. PCB Version change to A101-2
2. For customer design => Connect CB_PWR_EN to sus_s5#
3. Crystal Vender report => Change C586/C587 to 18p from 10p , C100/C101 to 10p from 1.2p , C565/C566 to 18p from 15p , R611 to 1.2k from 820ohm
4. For Freescale suggestion_RST > 500ms => Unmount R638 , POP C352
5. Avoid current leakage of +V5_IN => Reverse Q1602 , Change R1613 to 8.2k from 220k , R1622 to 1k from 47k
6. Fix the voltage of +V3.3_SB abnormal => Change R1665 to 22k , R1664 to 12k
7. Follow QSeven Spec , MCLK/RST/ENA are 1.8v level control signals => Add U1505~U1507/C1773 , Remove R670~R677/R681/R682 for space saving
8. For RX_CLK rise/fall time enhance => Change R190 to 10ohm from 22ohm
9. Design WDTO function for customer's required => Remove R86,R1704,R1705 ,TP49 , assign GPIO7_IO12 for WDTOUT function
10. For CMC's required => Change Y4 to 1231002776-01 from 1231002279-01
11. Avoid +V1.5_ddr ripple => Reserve C1774/C1775 (should close H4) , C1776 (Close L9)
12. For PWRBTN# Function => Reserve D1202
13. For customer's required => Add one USB Port.

ROM-7421 A101-3 PCB:19C6O74202-01, 96 BOM:9696O74200E Date: 2016/09/14

1. PCB Version change to A101-3
2. PWR OCP issue => Change R684 to 18k(OCP:7.95A) from 39k(OCP:>11A)
3. For current leakage of +V3.3_SB at AT mode => Change R1631 to NL , Add R1710 (10K) pull high to +v3.3_SB
4. For (Q1610) APL5327BI-TRG EOL, change to AP2127K-ADJTRG1(1410027429-01)
5. Change memory symbol, by CMC requset
6. Add D1202 for ATX power on / off

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