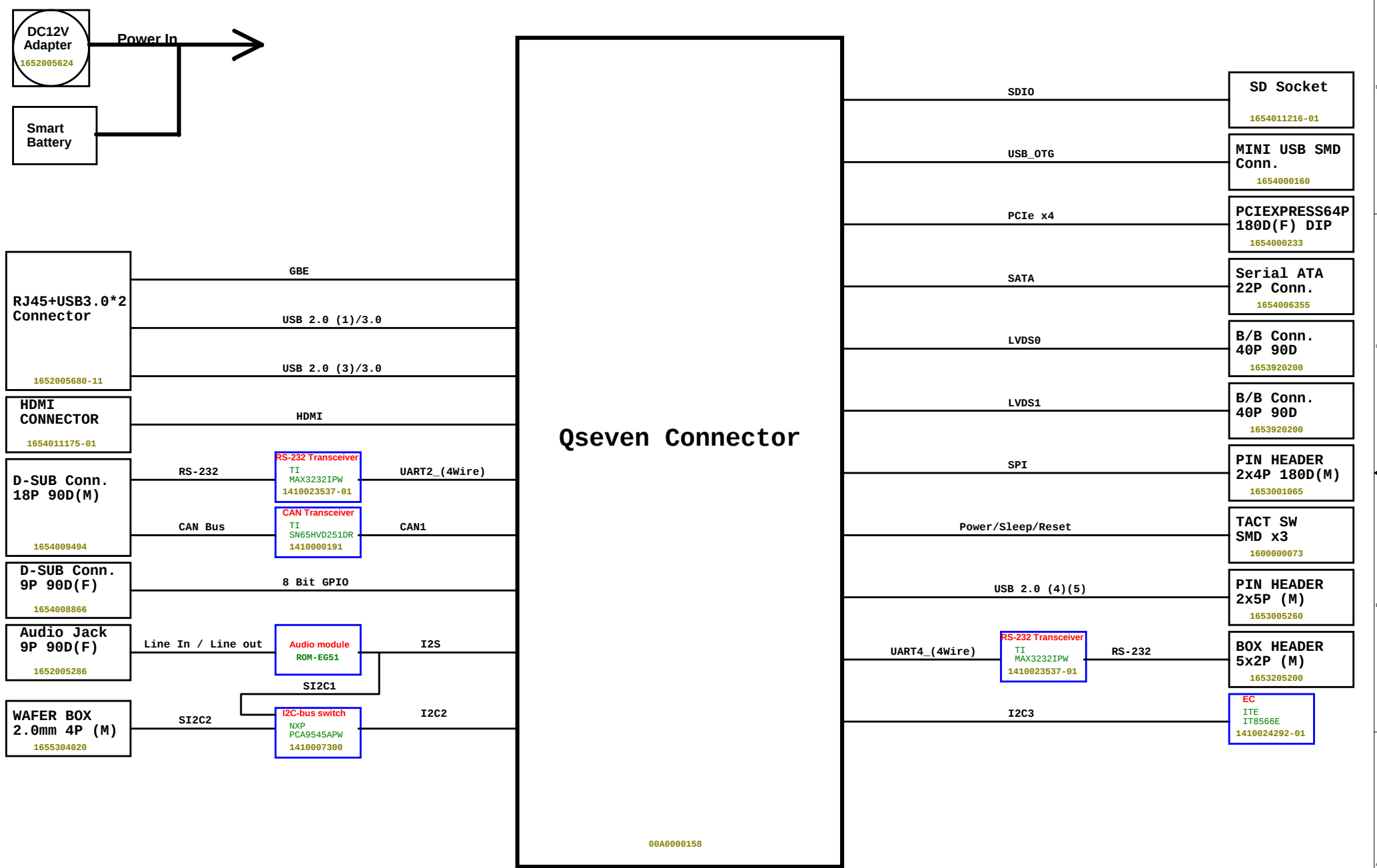


Model Name: ROM-DB7501 A101-2

01	COVER PAGE
02	HISTORY
03	BLOCK DIAGRAM
04	POWER BLOCK DIAGRAM
05	POWER ENABLE SEQUENCE
06	DC IN / +V1.8
07	BATTERY CHARGER
08	+V3A / +V5A / +V3 / +V5
09	+V12
10	LVDS0
11	LVDS1
12	HDMI
13	USB 3.0 & OTG
14	GigaLAN
15	PCI-E
16	SATA, SDIO, JTAG
17	CAN BUS
18	COM
19	I2S & Audio
20	SPI, I2C, LED, GPIO
21	BUTTON
22	EC
23	QSEVEN_MXM CONNECTOR

1. Initial Release

- 01. PCB P/N change to 19A6750101-01
- 02. Can't turn off +V5 issue => Change the power source of U10.pin4 to +V3A from +V3
- 03. CARRIER_PG00D should drive to low level first than any power source down => Mount Q20 , Change R90 to 43k
- 04. PowerOn sequence turning => Change R96 to 47k from 240k , R63 to 8.2k from 100k , Mount C34
- 05. OTG_USB Power can't turn on issue => connect USB_OTG_PWREN to U3.pin3
- 06. SD Power can't turn on issue => Add Q51/R411 , Mount R65
- 07. The voltage level of +V5 is not enough when batt mode => Unmount R73,R67 , Add R383,R384
- 08. RTS/CTS function abnormal => Swap RTS & CTS connection.
- 09. Follow ISO-11898/11519 _ CAN Bus Description => Correct the pin definition of CAN Bus on D-SUB9 , Reserve PS3
- 10. Avoid LAN's current leakage => Unmount R331,R341
- 11. Avoid CPU can't detect SD Card insert or not , when the power of +V3_SDIO is turn off . => Unmount R21 , Add R390
- 12. Follow DFM report indicate the Naming Rule of Jumper , correct the PartReference => ATATX1(1-2)1,LVDS_VDD1(1-2)1,LVDS_BL1(1-2)1.....
- 13. LCD_BKLT_EN & LCD_BKLT_PWM have glitch before POR# de-assert => Add Q52-Q54,R392,R393
- 14. TPS51125 Continue mode for +V3A/+AVCC ripple issue => Add R394
- 15. For PCIe CLK rise/fall time issue => Remove R167/R161
- 16. For EMI & CLK Overshoot issue => Add 22p on AUDIO_MCK , Bead for OSC PWR , C224-C226 , R395/R396 , Unmount D42-D44/R357 , Change B33-B35 to 1k from 60ohm
- 17. Design WDTO function for customer's required => Add R397/D58
- 18. Avoid current leakage from WDT_TIME_OUT# => Add R398/D59
- 19. For CMC's required => Update MXM connector symbol , Change D46/D47 to 1300005439-01 from 1300000473
- 20. Naming => Rename CN22 to SATADOM_PWR1
- 21. Add one USB port for customer's required => Add one USB port & Power solution.
- 22. change R78 to 19.6k from 20k, by USB drop issue.



ATX Mode

+VDC_SYS

+V5A

+V3A

+V1.8A

PWRBTN

CARRIER_PWR_ON

+V12

+V5

+V3

+V1.8

CARRIER_PG00D

RESET_OUT

+VDC_SYS to +V5A > 0ms

+VDC_SYS to +V3A > 0ms

+V3A to +V1.8A > 0ms

+V1.8A to PWRBTN > 0ms

PWRBTN to CARRIER_PWR_ON > 0ms

CARRIER_PWR_ON to +V12 > 0ms

CARRIER_PWR_ON to +V5 > 0ms

CARRIER_PWR_ON to +V3 > 0ms

+V3 to +V1.8 > 0ms

+V1.8 to CARRIER_PG00D > 0ms

CARRIER_PG00D to RESET_OUT > 0ms

ADVANTECH

Title POWER ENABLE SEQUENCE

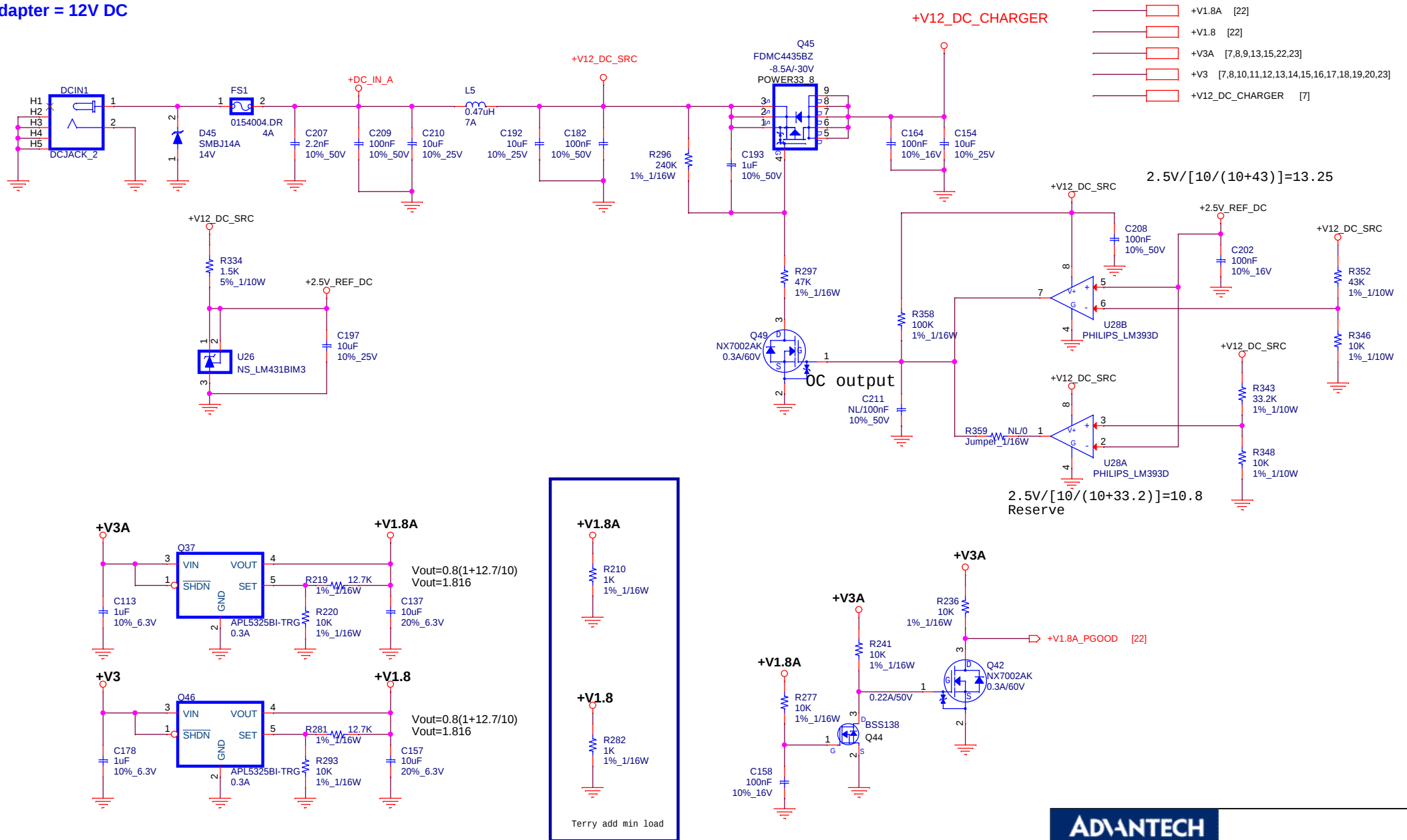
Size Document Number ROM-DB7501

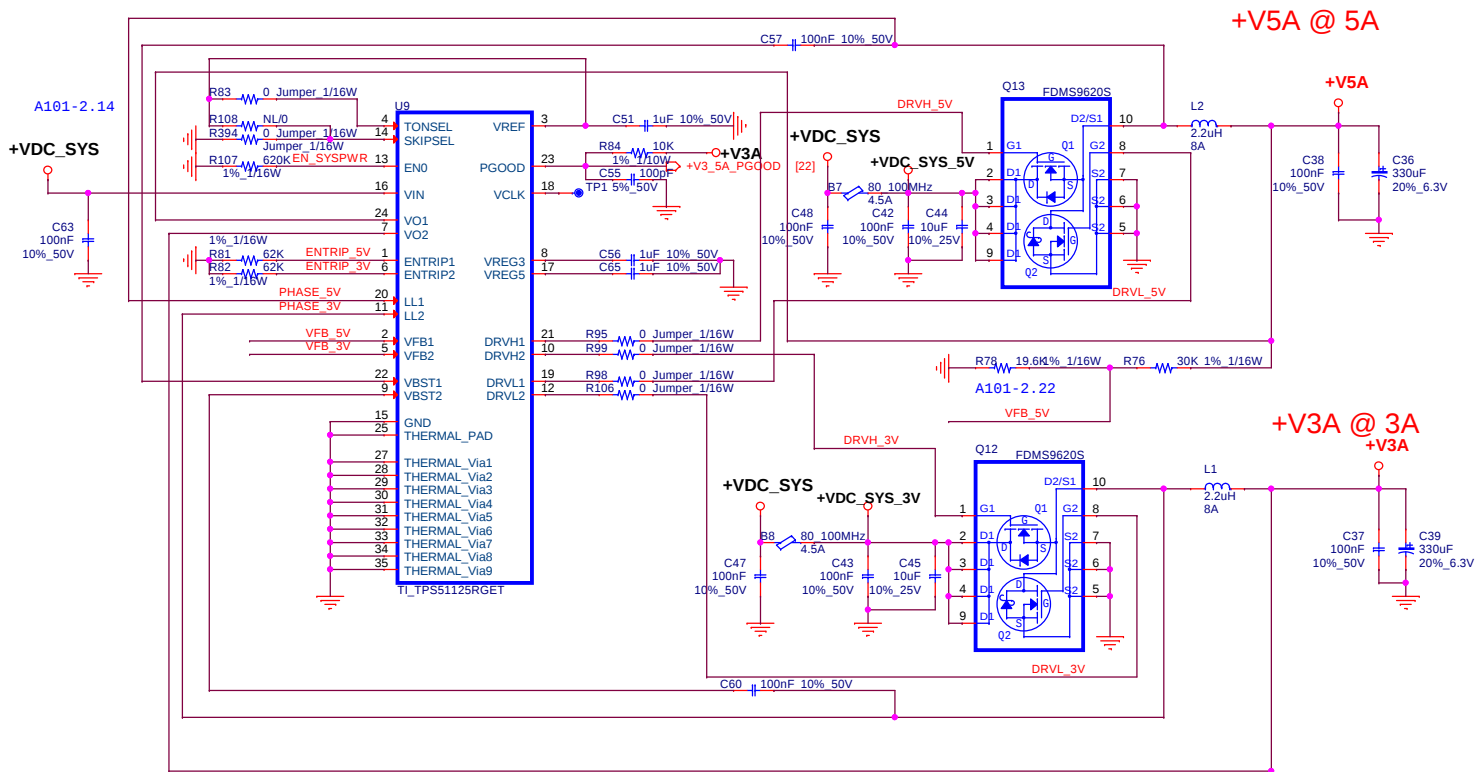
Date: Tuesday, October 04, 2016

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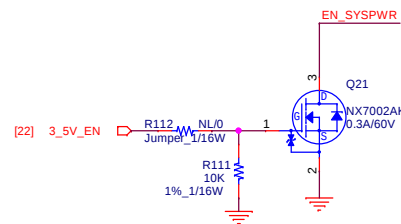
Rev A101-2

Adapter = 12V DC





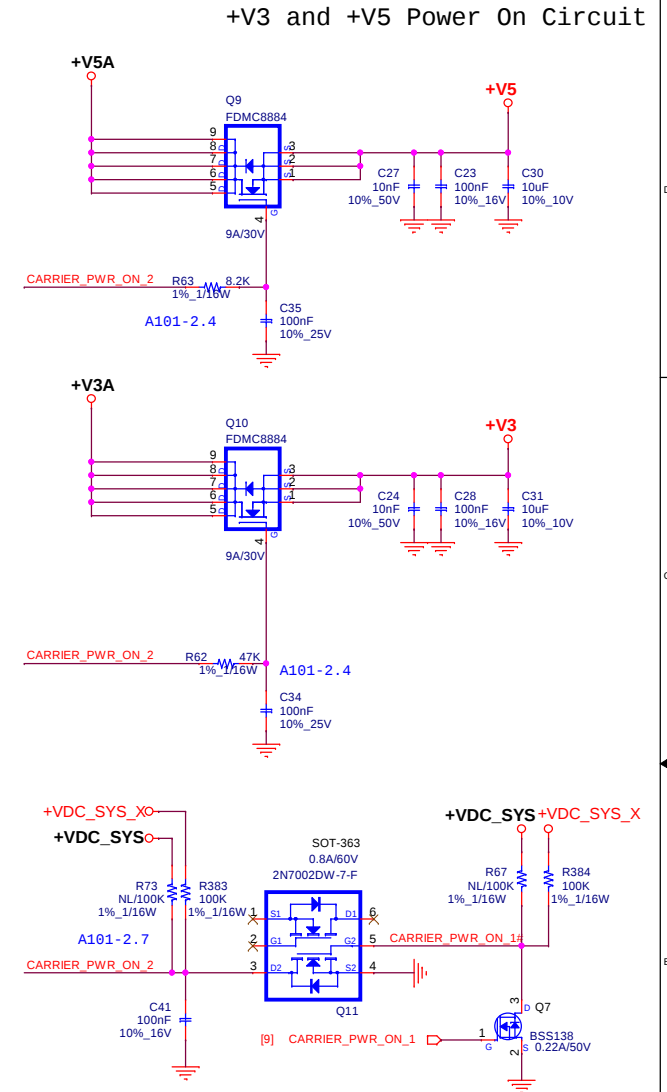
EN0 is the control pin of VREG5, VREG3 and VREF regulators



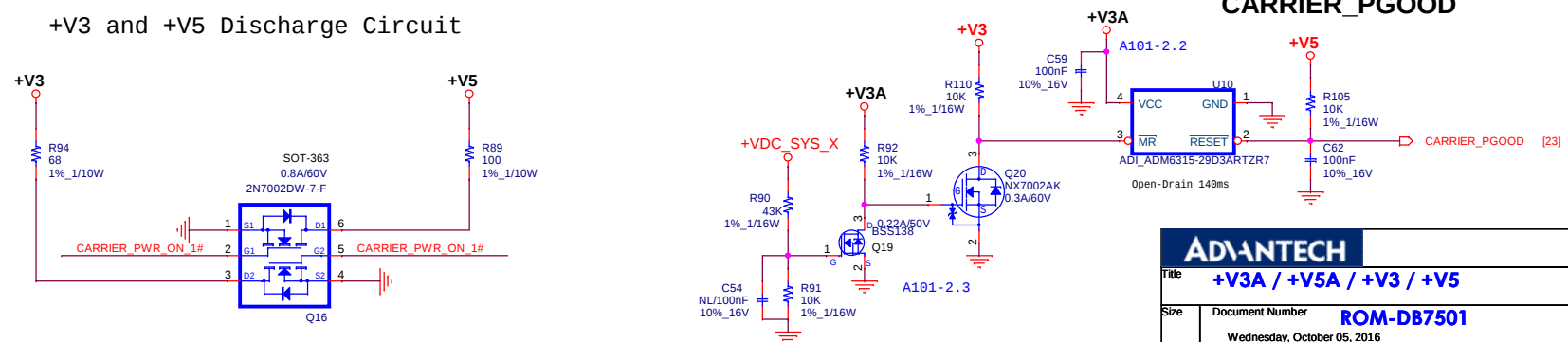
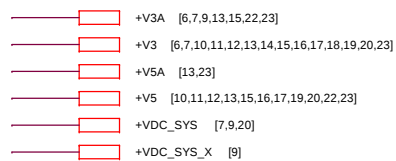
$$V_{TRIP} \text{ (mV)} = \frac{R_{TRIP} \text{ (k}\Omega) \times I_{TRIP} \text{ (}\mu\text{A)}}{9} - 24 \text{ (mV)}$$

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

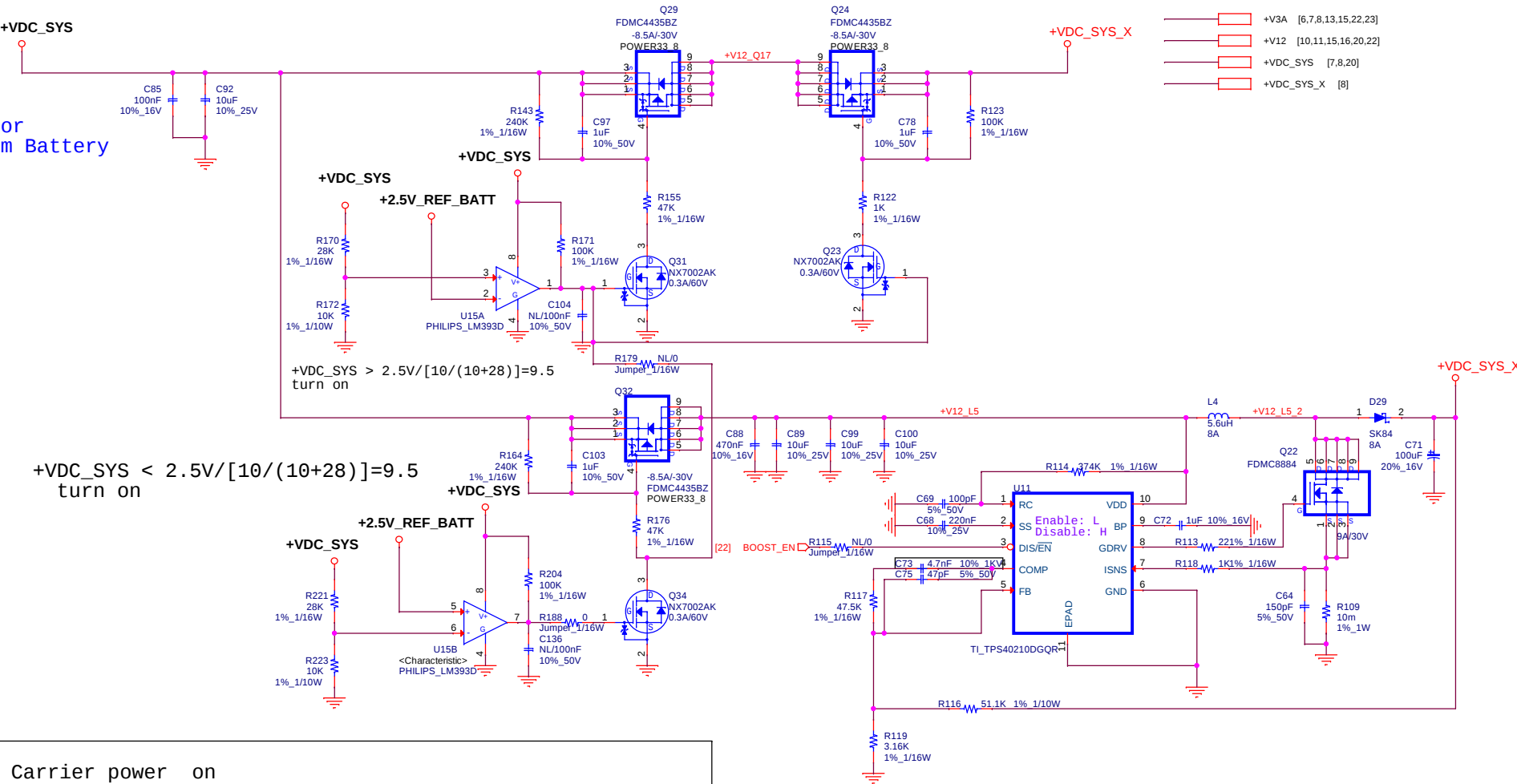
```
+V3A I limite ~ 6.78A +/- 10%
+V5A I limite ~ 6.78A +/- 10%
```



+V3 and +V5 Discharge Circuit

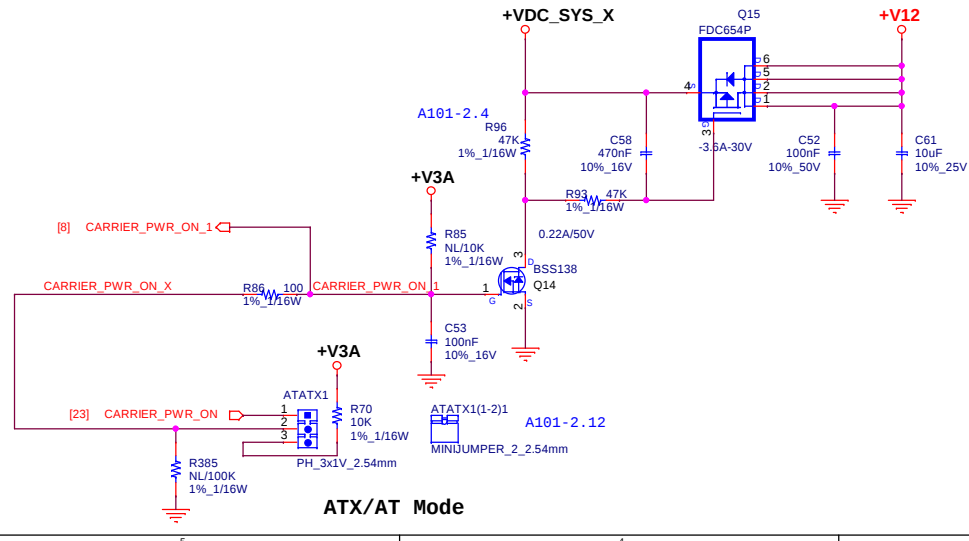


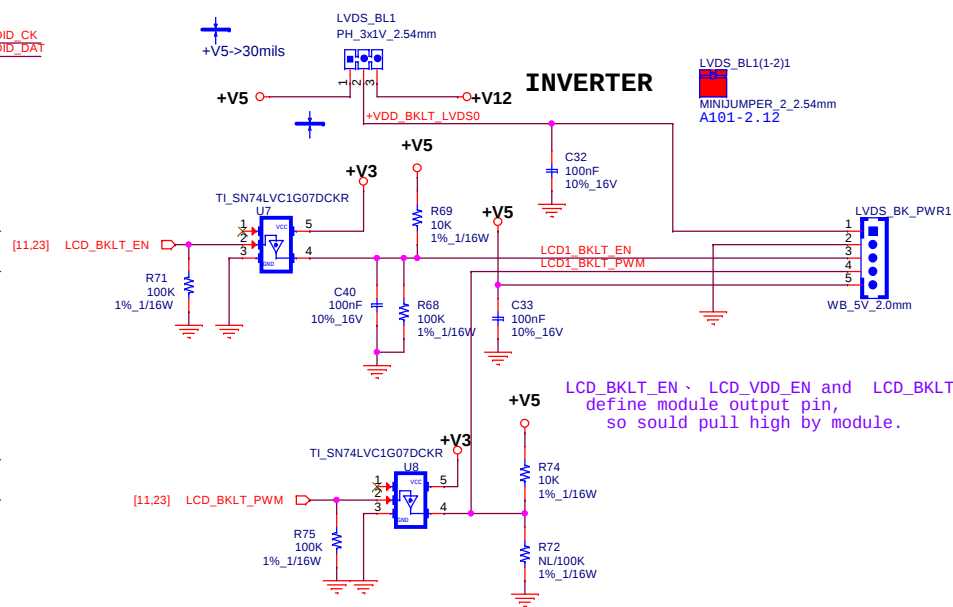
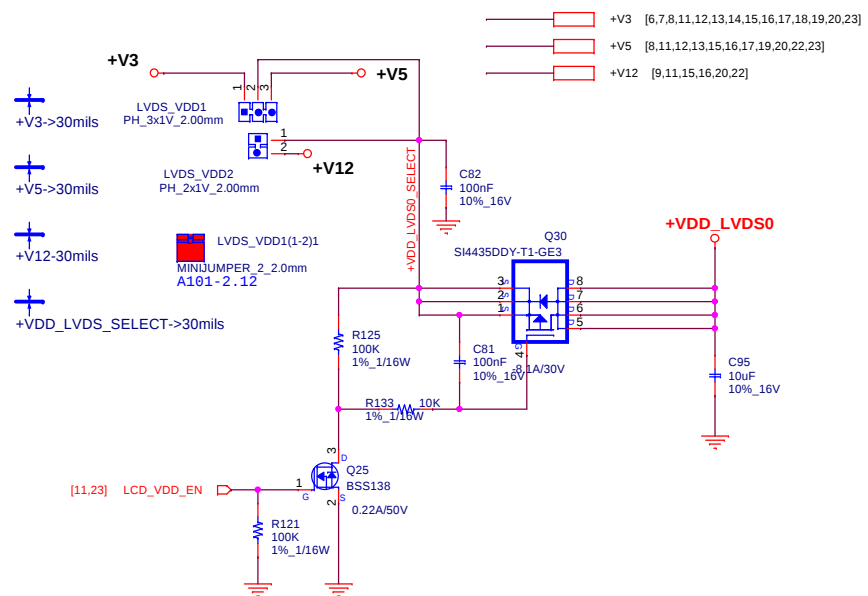
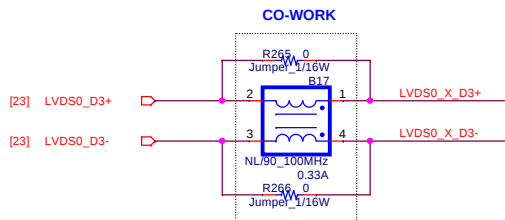
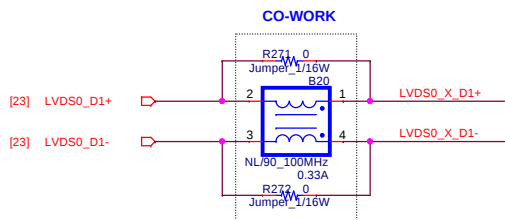
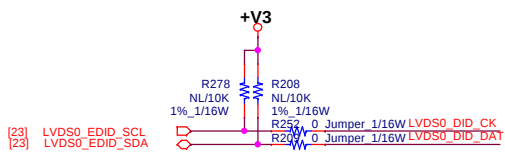
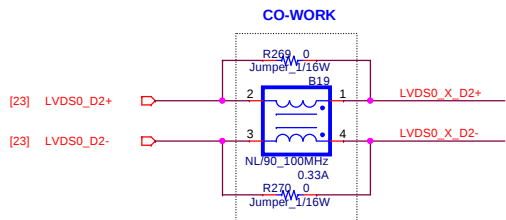
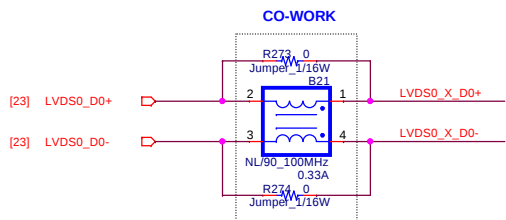
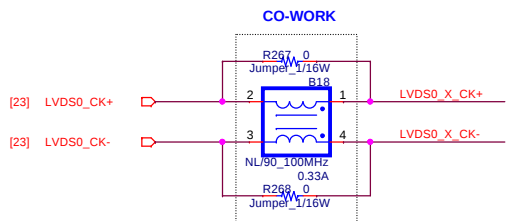
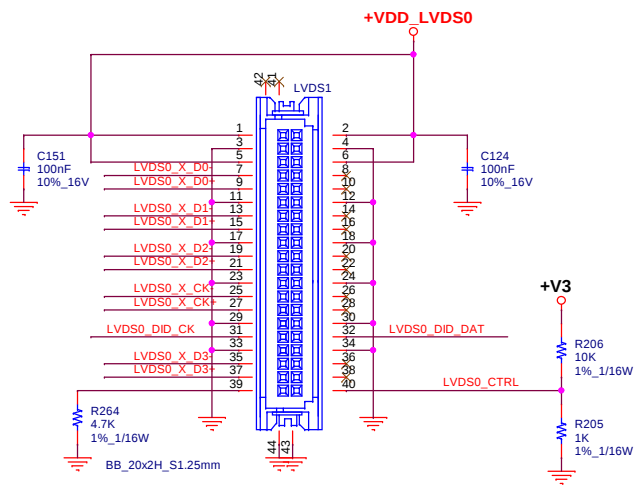
This circuit is for power source from Battery



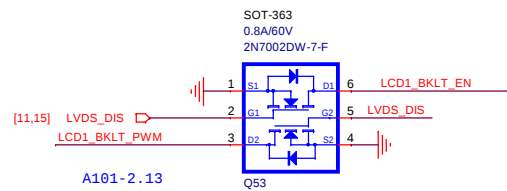
+VDC_SYS < 2.5V/[10/(10+28)]=9.5
turn on

Carrier power on

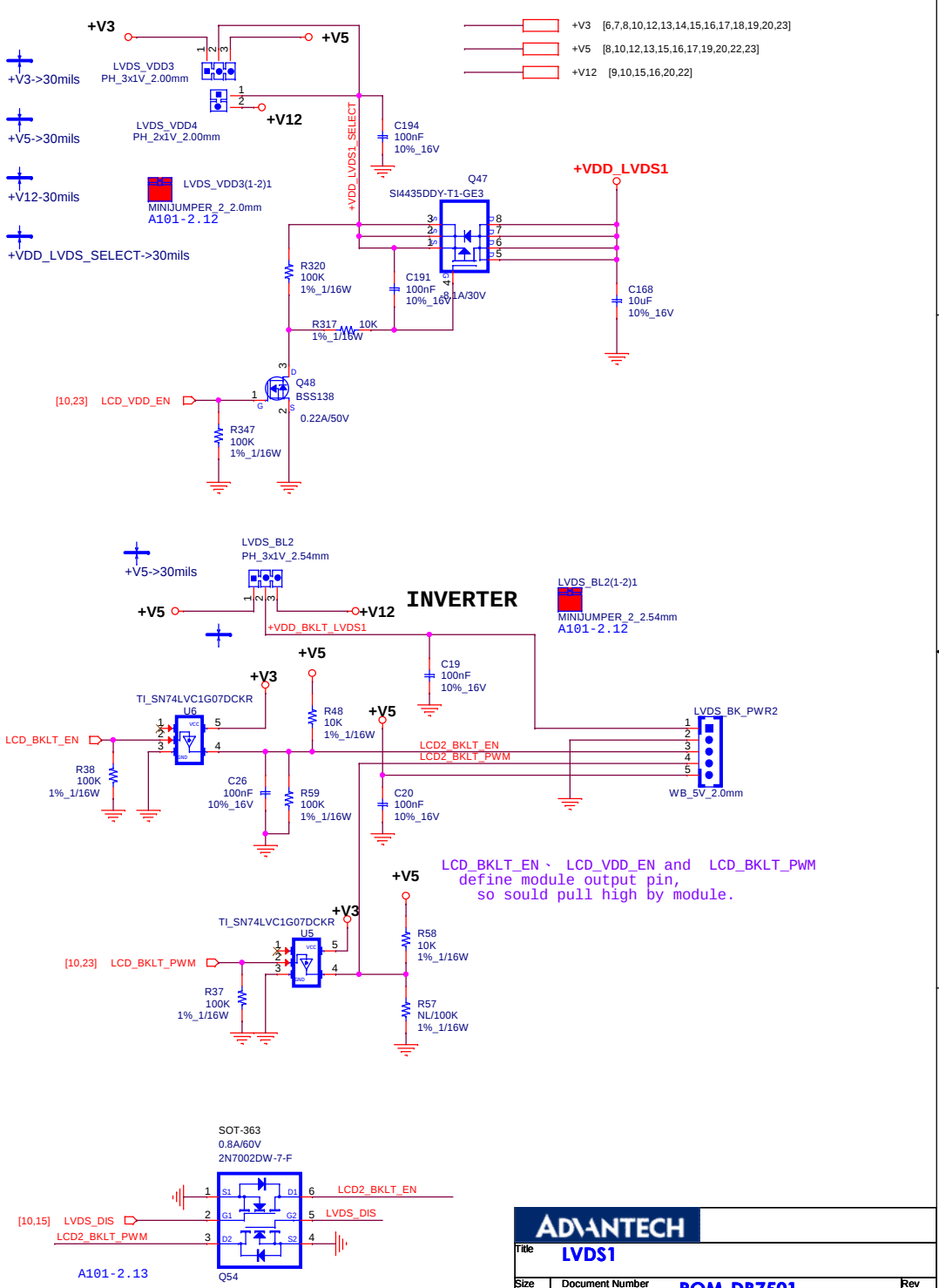
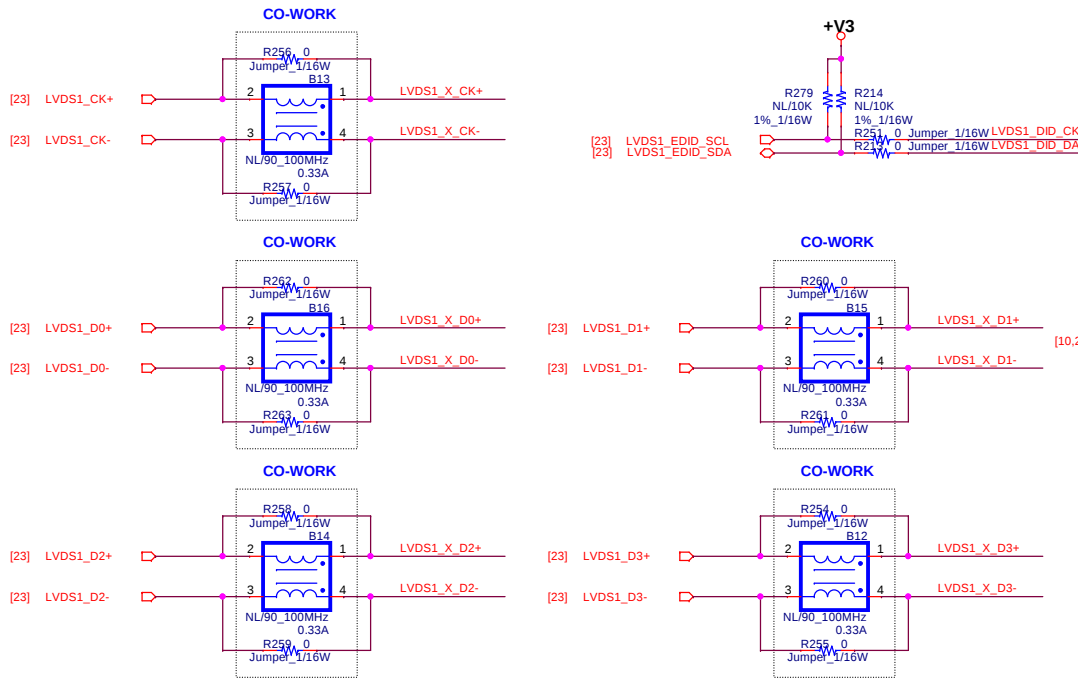
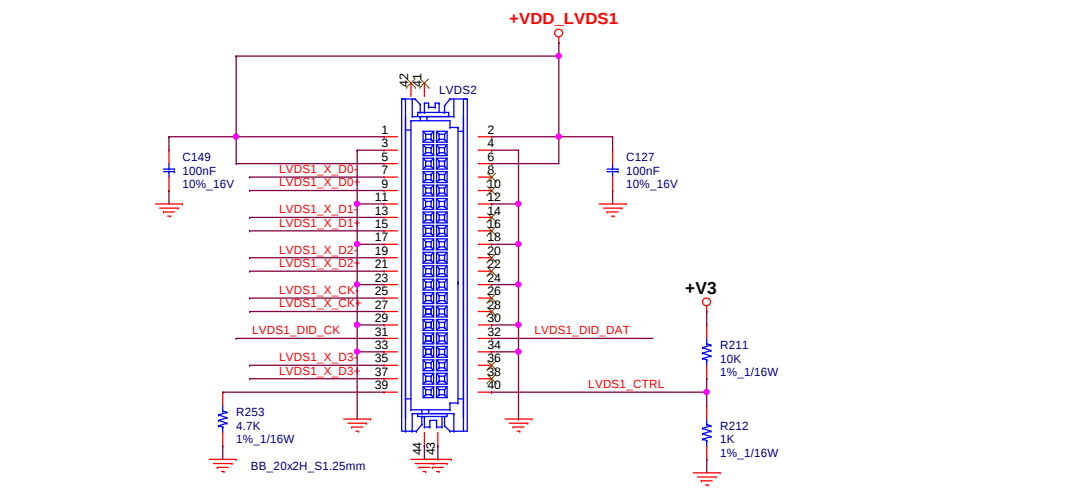


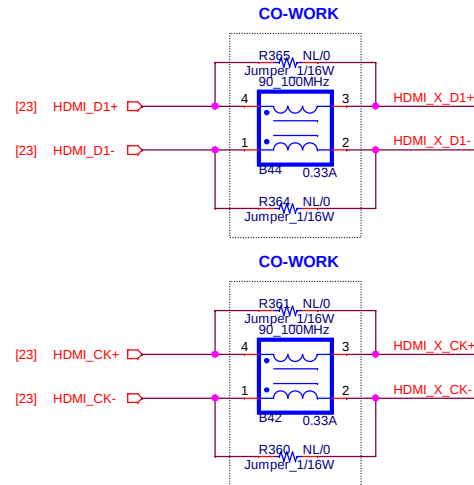
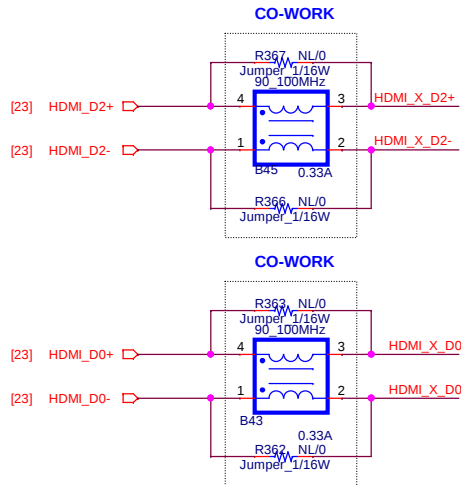


LCD_BKLT_EN、LCD_VDD_EN and LCD_BKLT_PWM define module output pin, so could pull high by module.

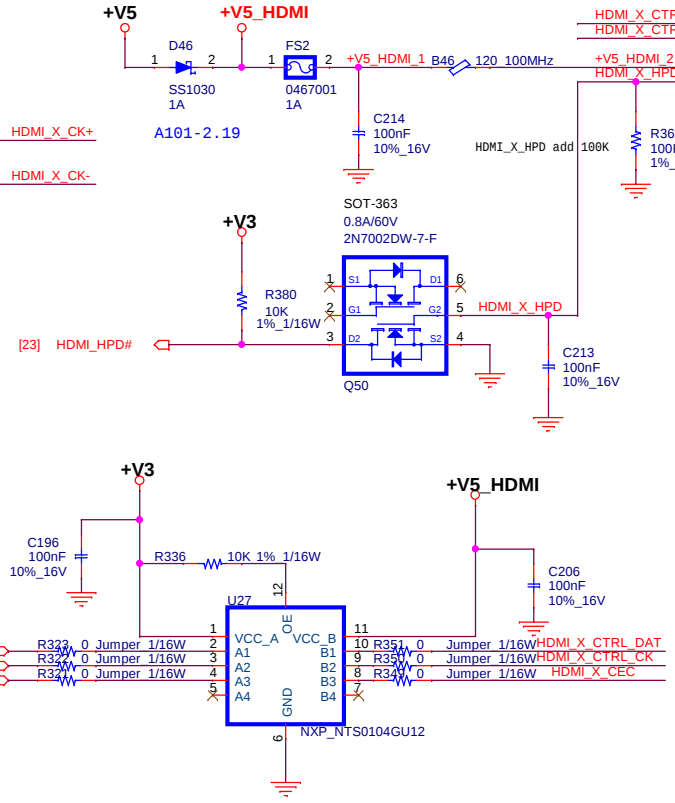
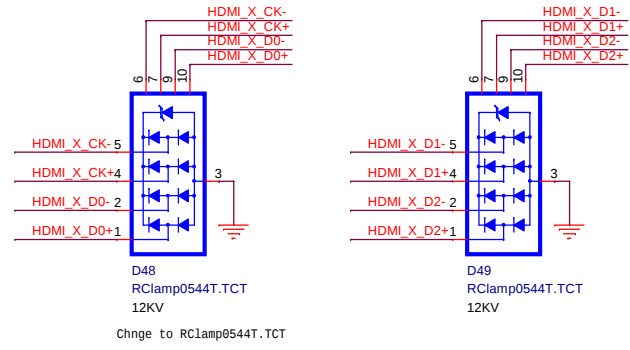


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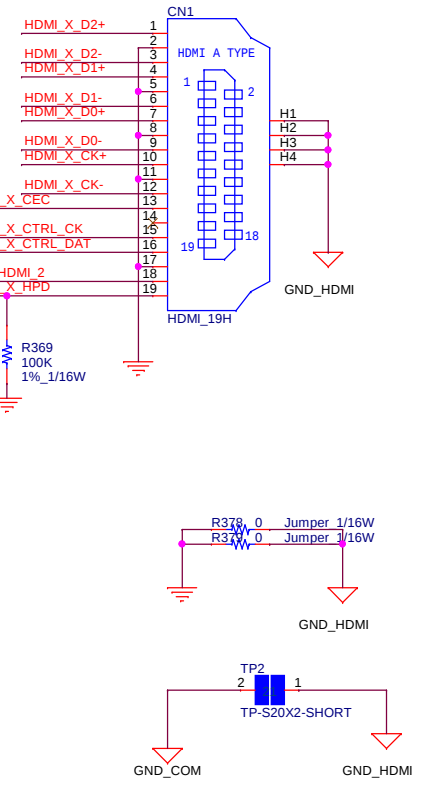




Close to HDMI connector



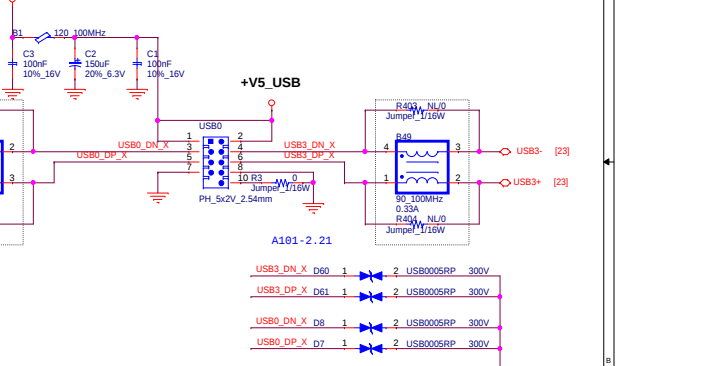
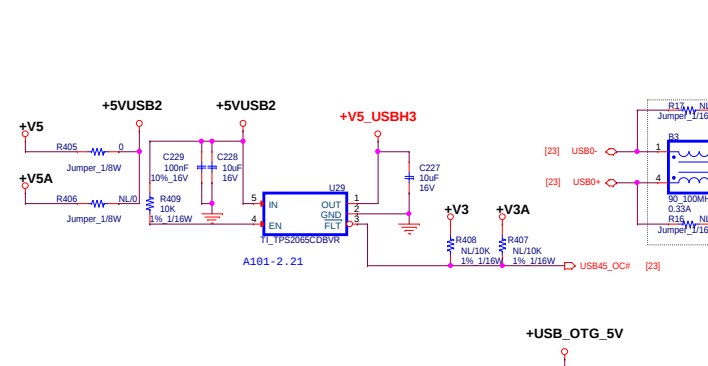
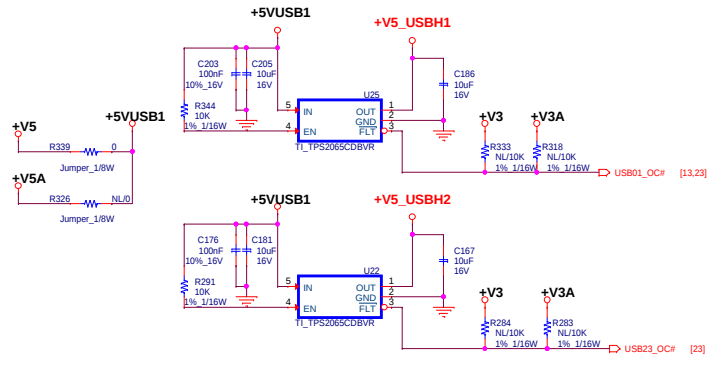
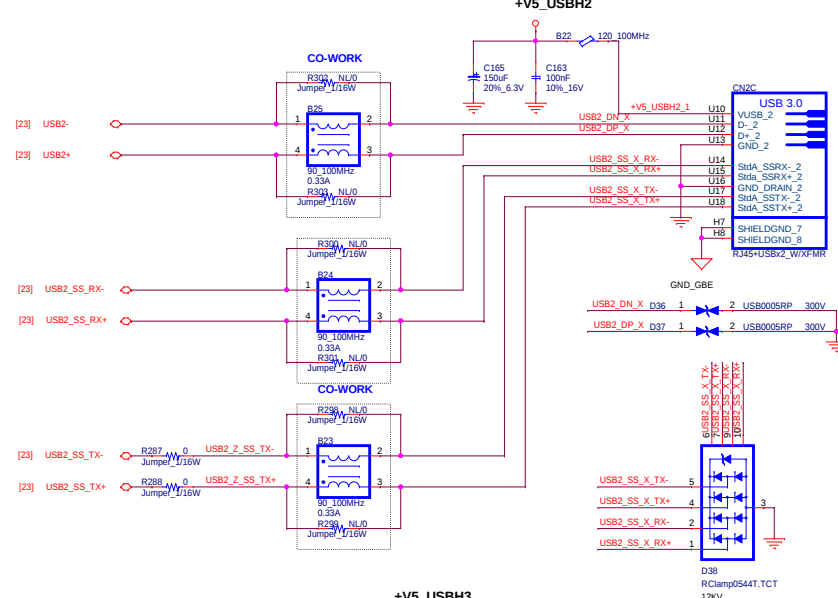
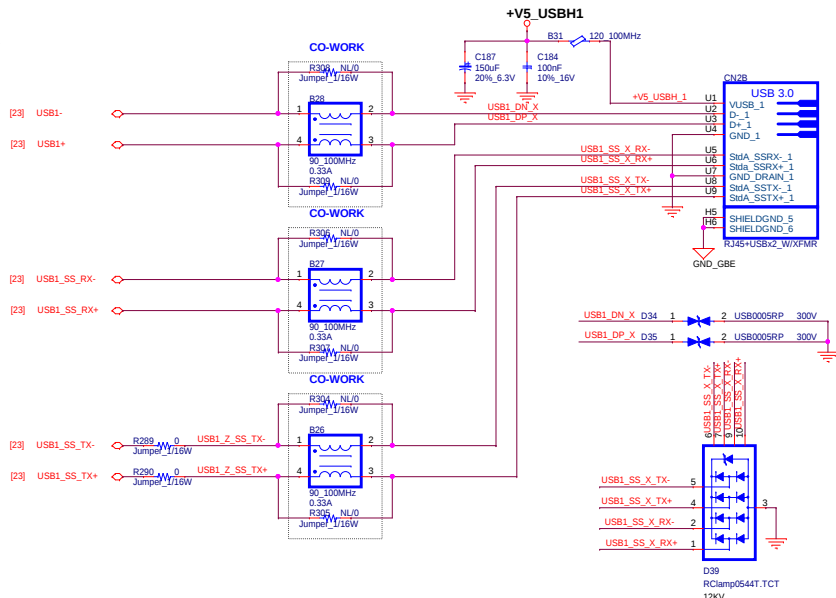
+V3 [6,7,8,10,11,13,14,15,16,17,18,19,20,23]
+V5 [8,10,11,13,15,16,17,19,20,22,23]



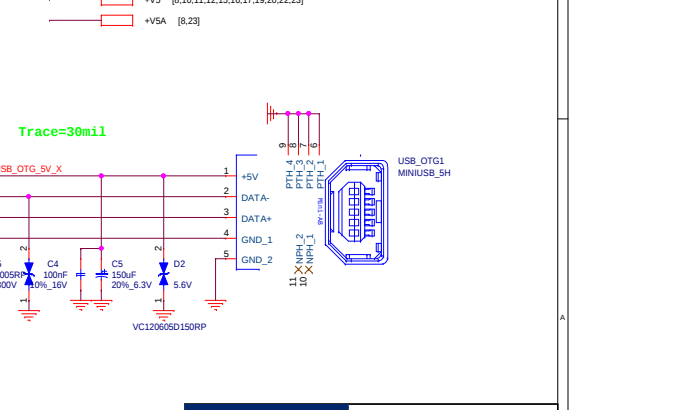
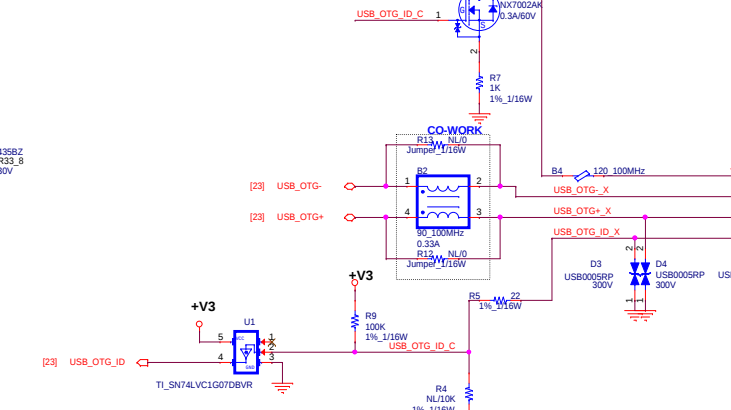
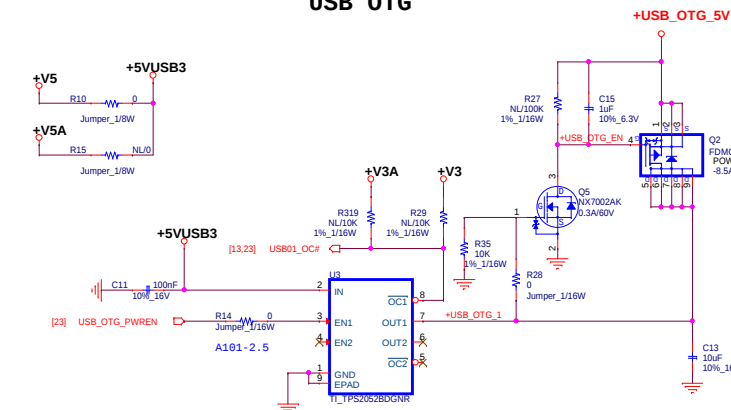
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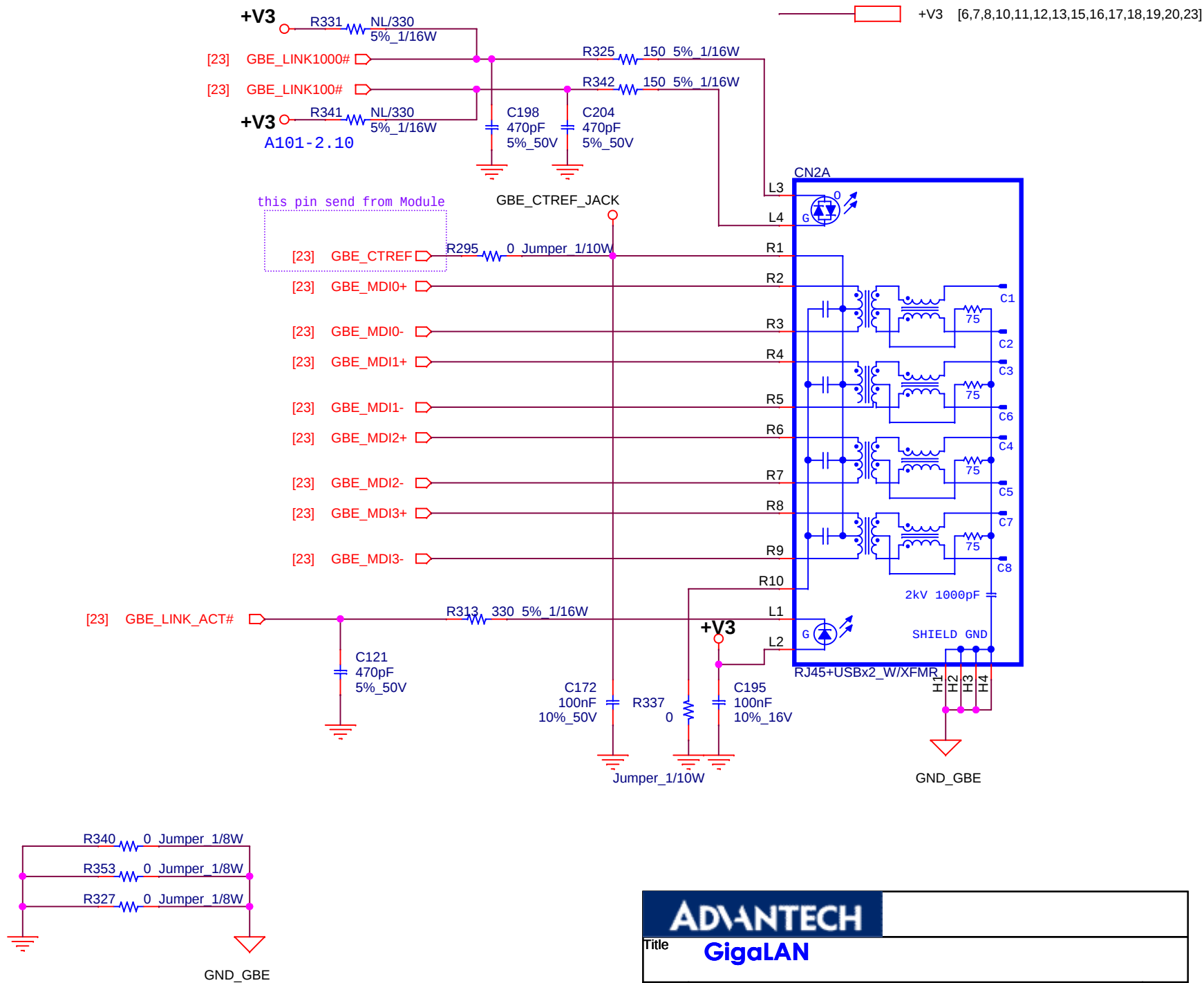
A101-2

USB HOST



USB OTG





ADVANTECH

Title **GigaLAN**

Size

Document Number

ROM-DB7501

Rev

A101-2

Date:

Tuesday, October 04, 2016

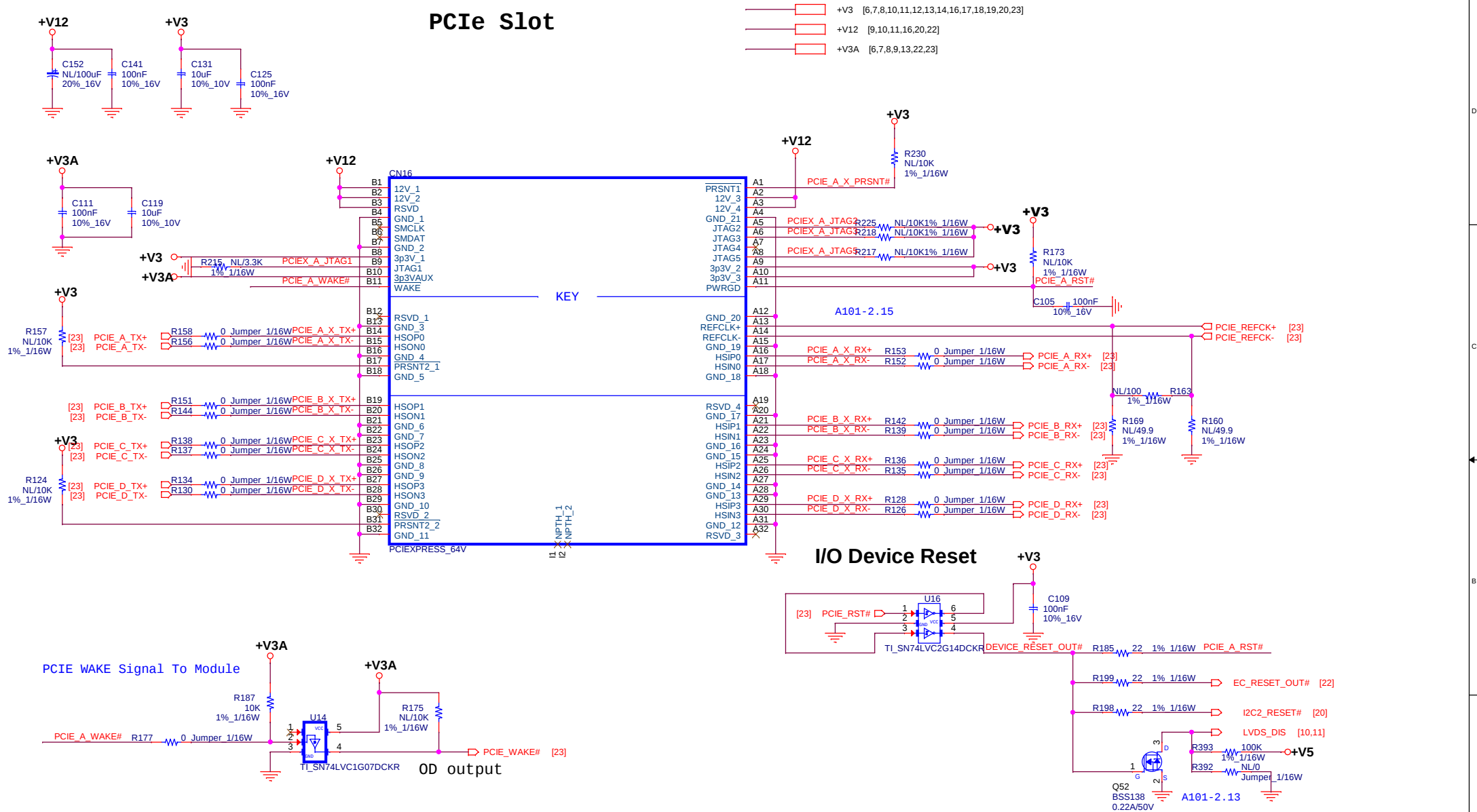
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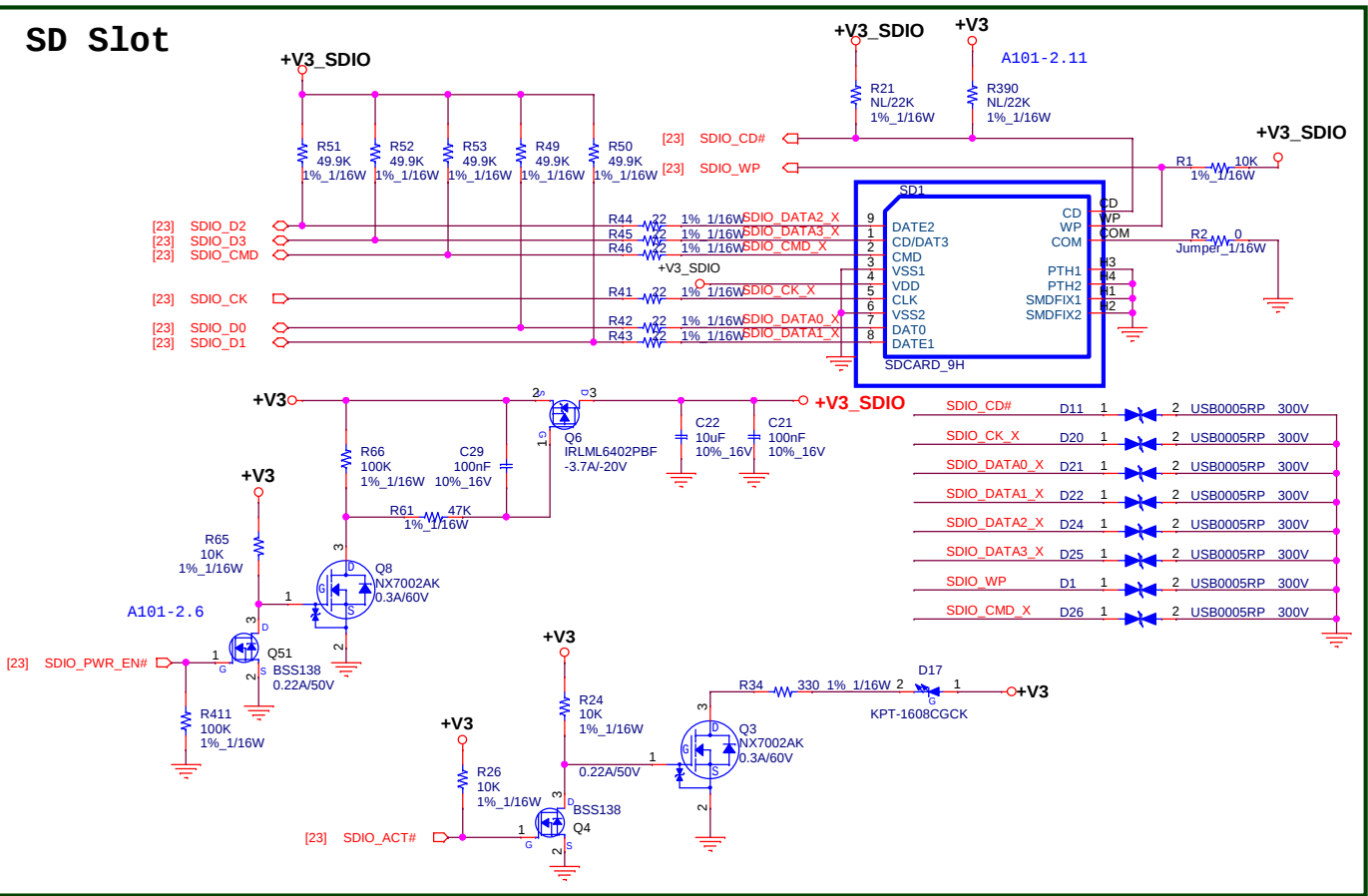
23

PCIe Slot

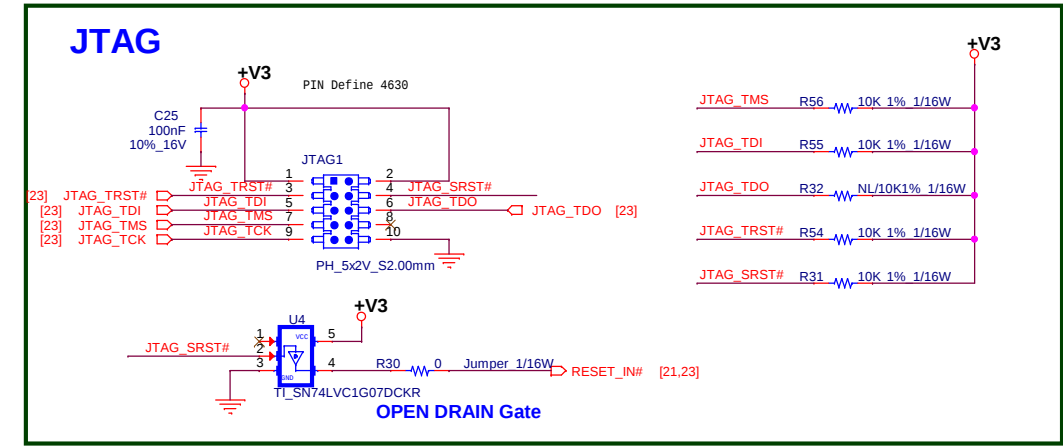


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SD Slot

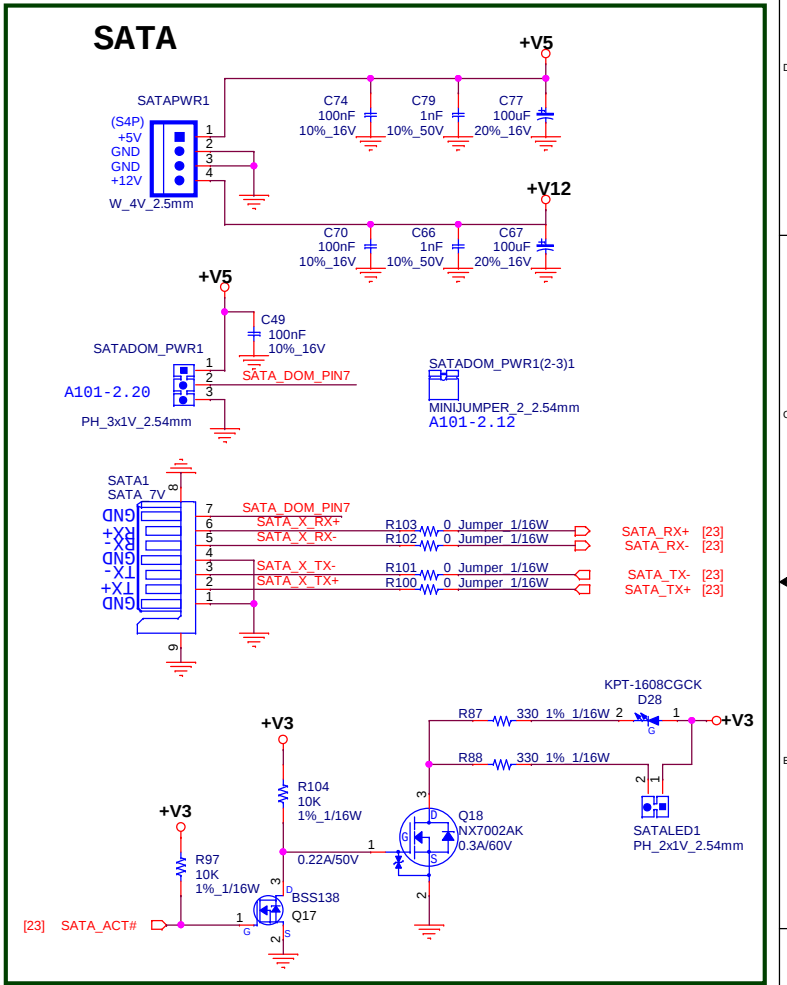


JTAG

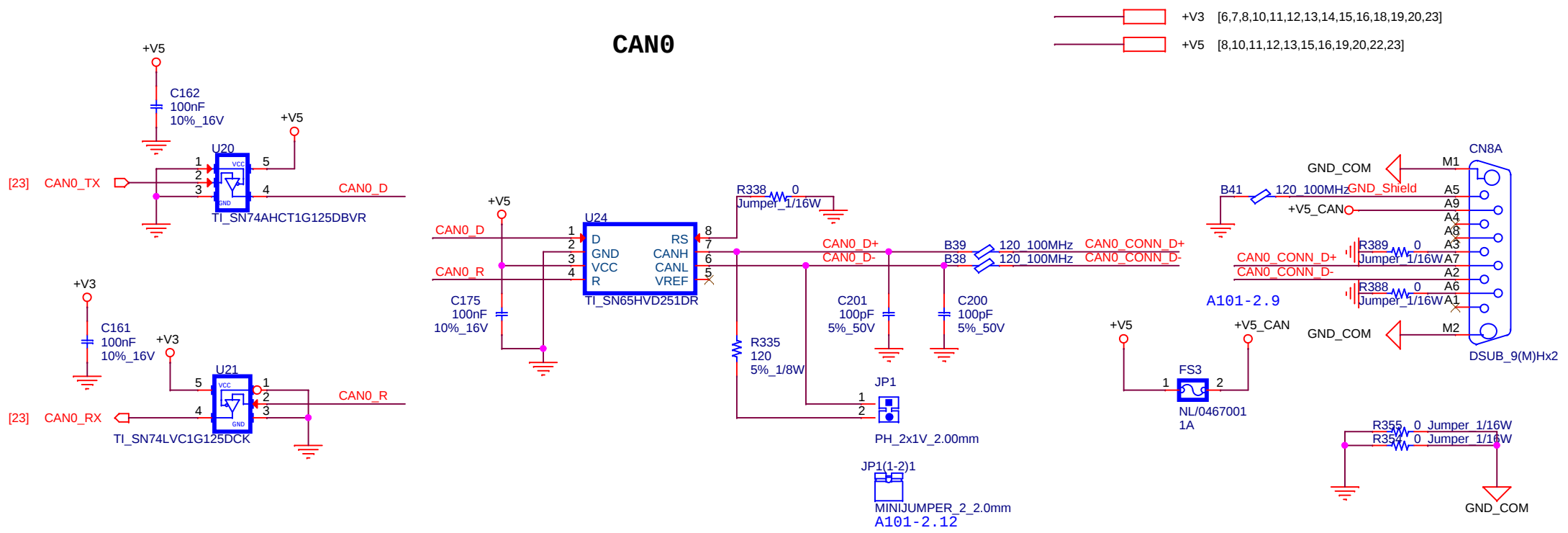


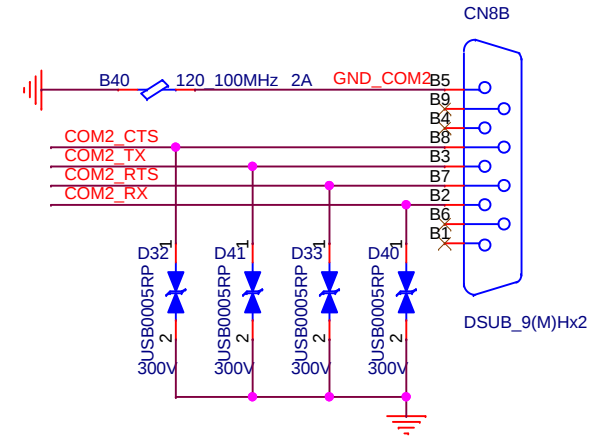
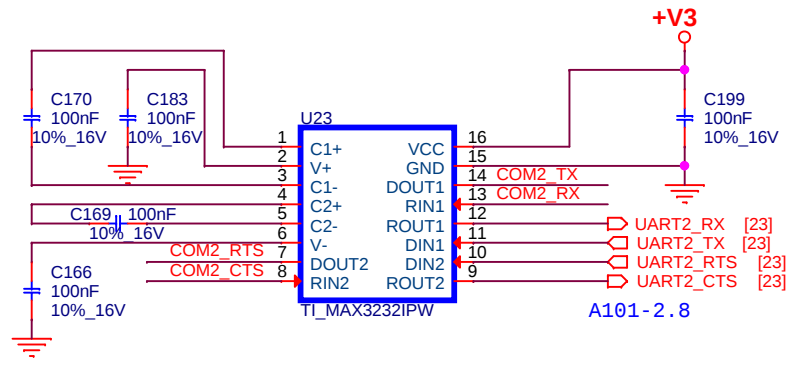
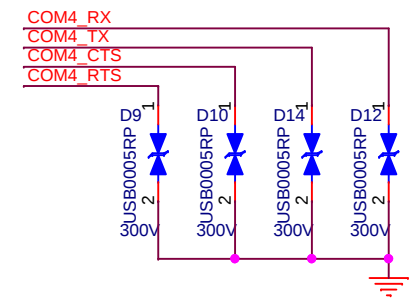
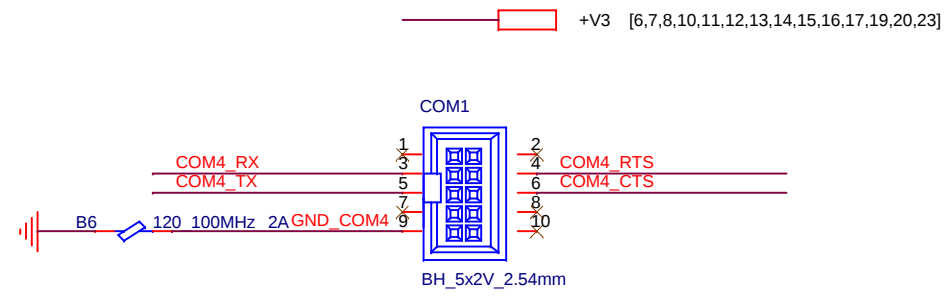
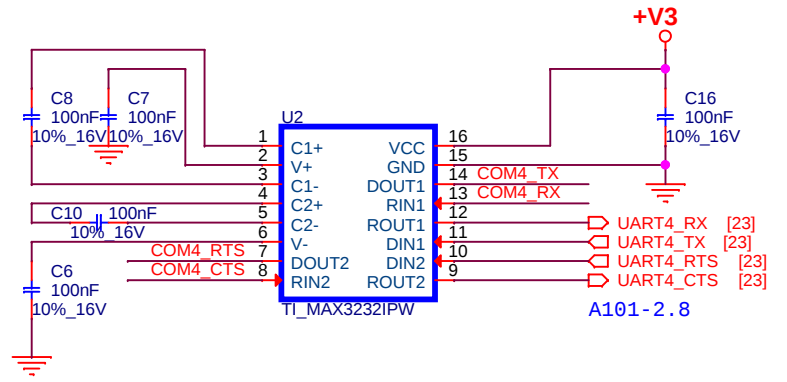
- +V3 [6,7,8,10,11,12,13,14,15,17,18,19,20,23]
- +V5 [8,10,11,12,13,15,17,19,20,22,23]
- +V12 [9,10,11,15,20,22]

SATA

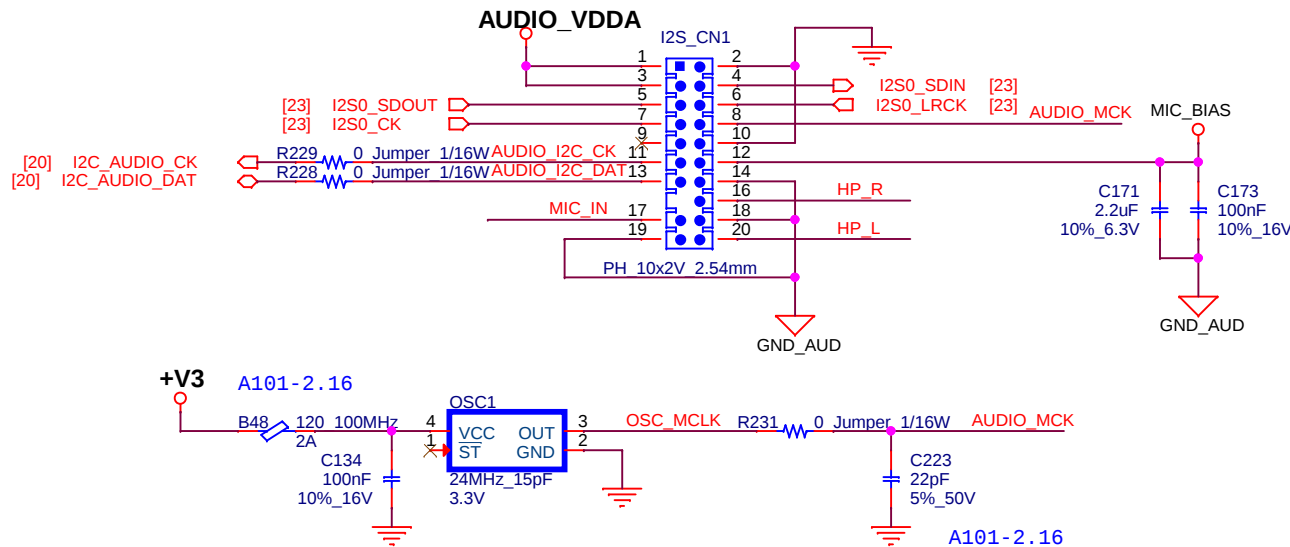


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Title	SATA, SDIO, JTAG		
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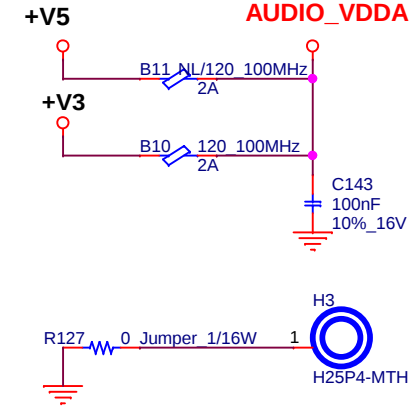
I2S0 connect to CODEC



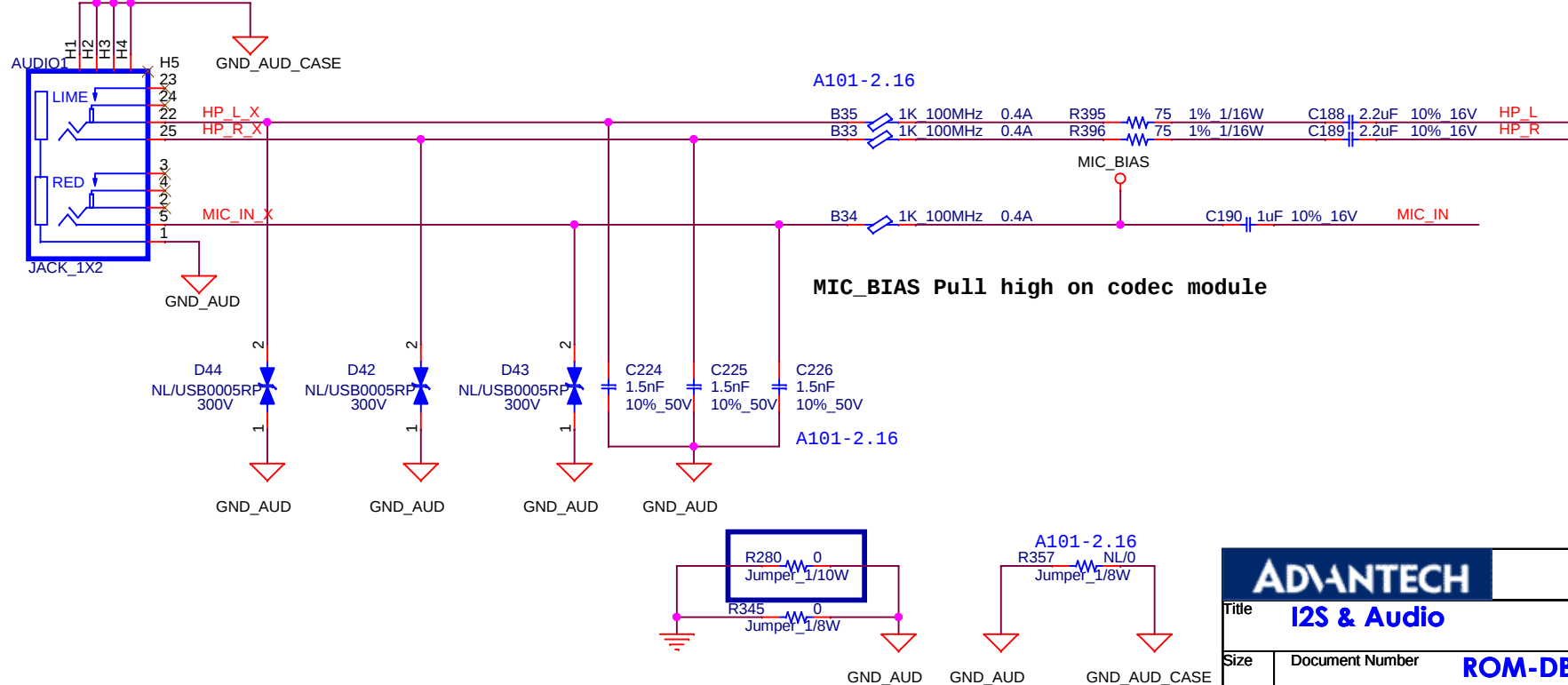
+V3 [6,7,8,10,11,12,13,14,15,16,17,18,20,23]

+V5 [8,10,11,12,13,15,16,17,20,22,23]

Audio Power



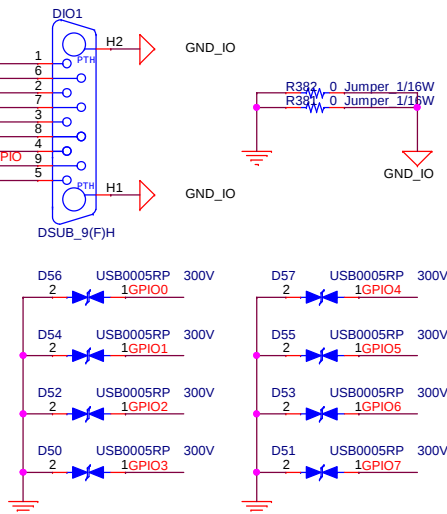
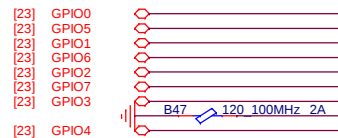
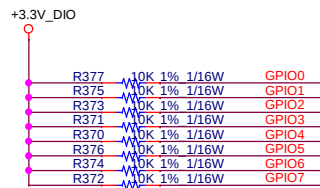
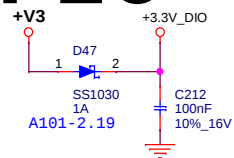
Phone JACK



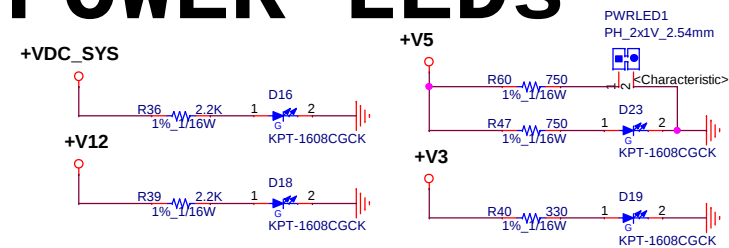
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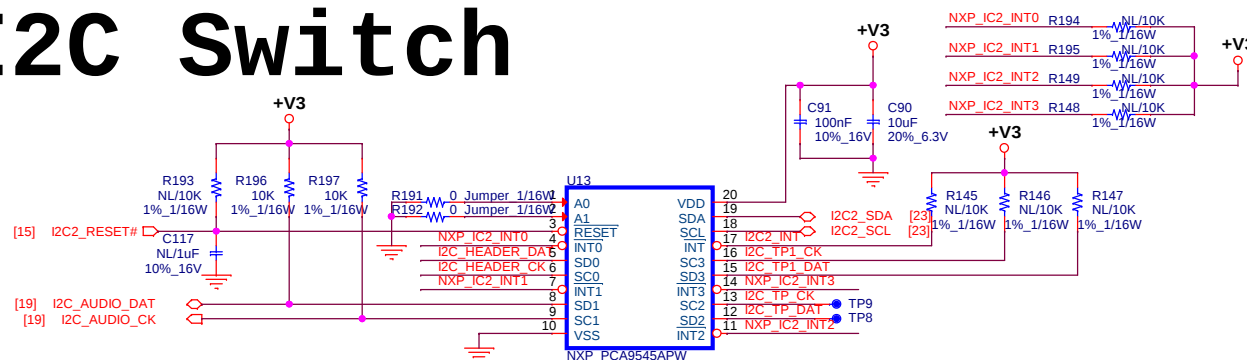
GPIO



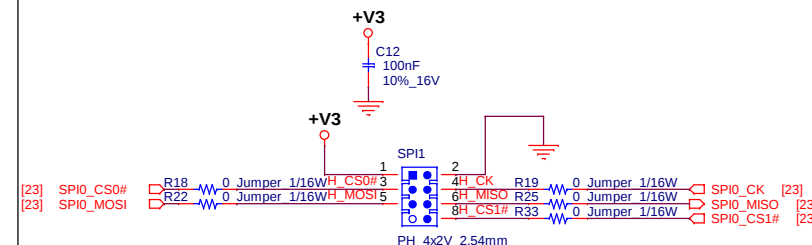
POWER LEDs



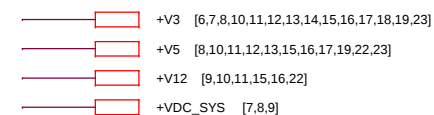
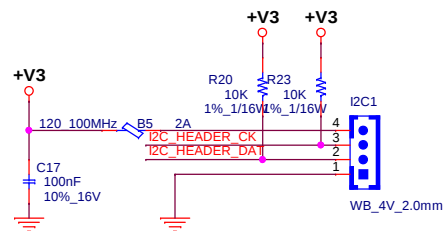
I2C Switch



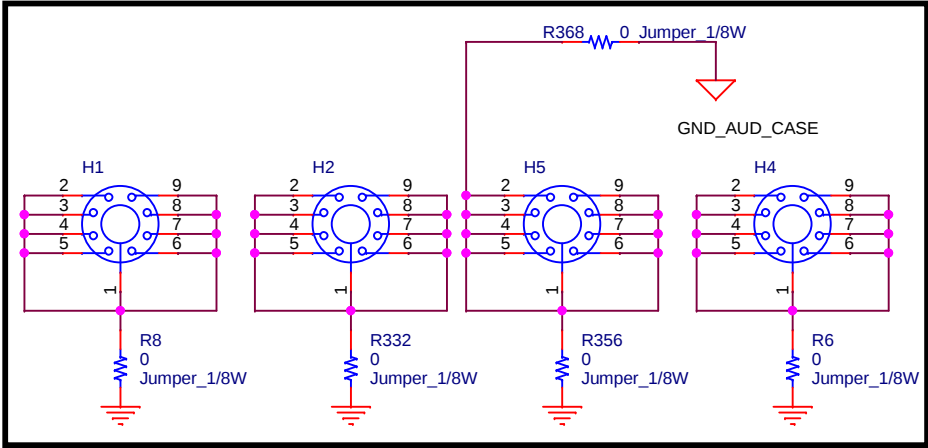
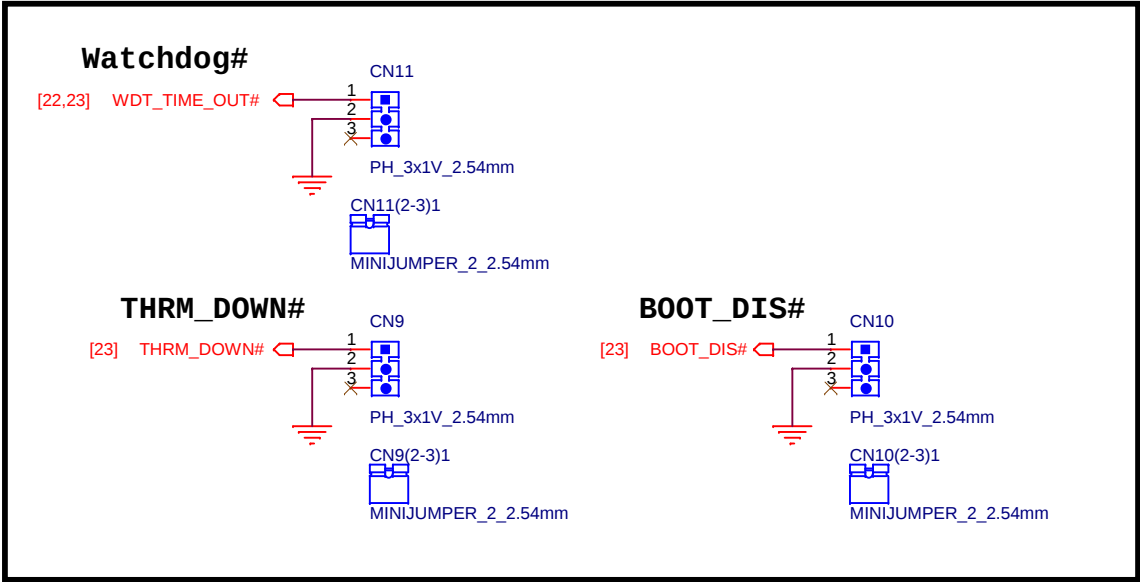
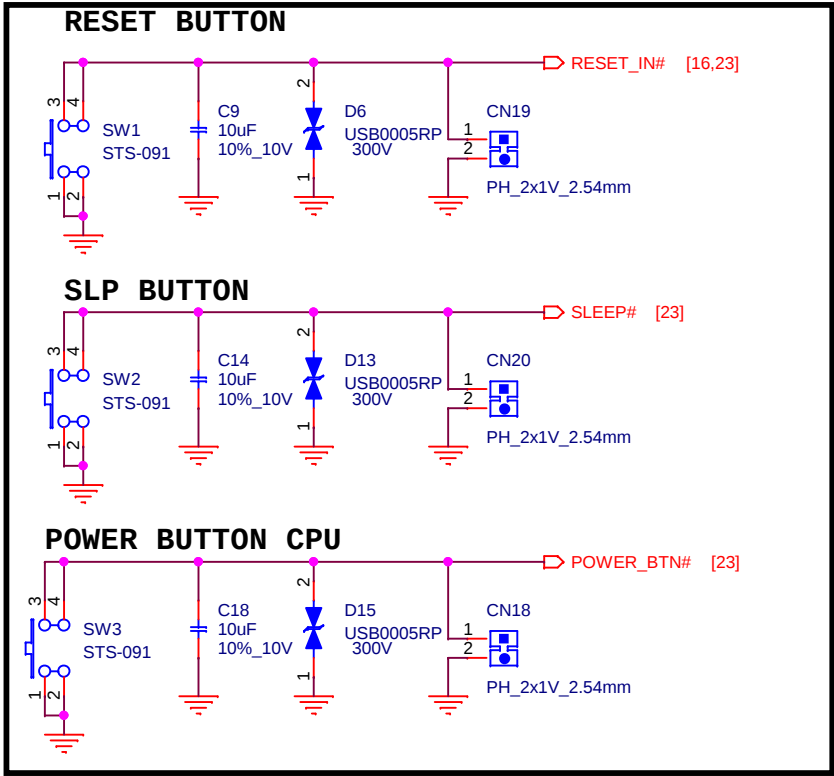
SPI CONNECTOR

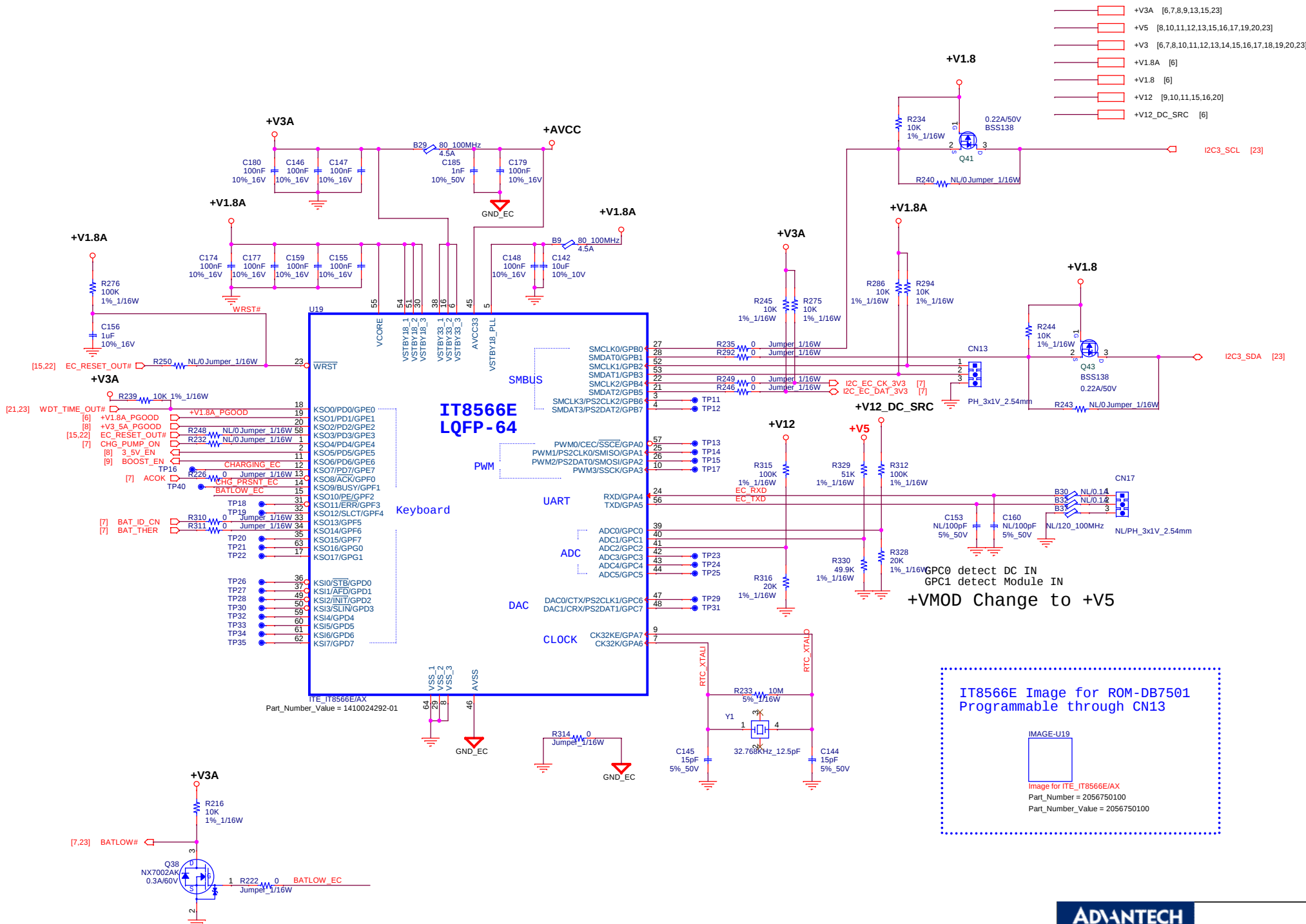


I2C Header



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CHARGING_EC: High Charging, Low without charging
 CHG_PRSNT_EC: High Charger inserted, Low No charger inserted
 BATLOW_EC: High Battery low

