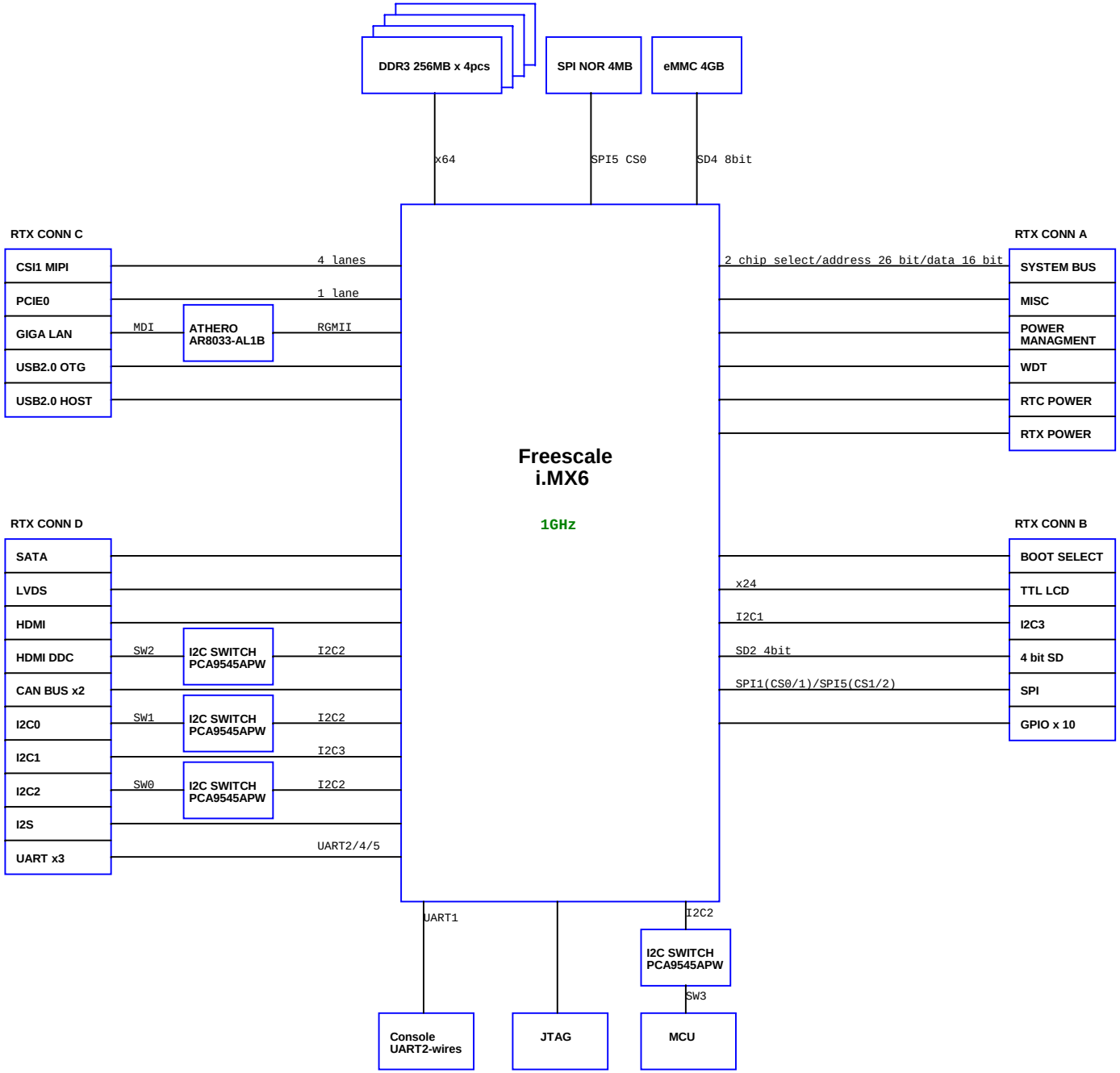
DESCRIPTION	PAGE
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Power Block Diagram	3
Power Enable Sequence	4
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iMX6 I/O-2	6
iMX6 I/O-3	7
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eMMC / SPI ROM / MCU	11
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GIGA LAN	13
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ROM-3420
A101-4

ADVANTECH

Title: Title Page		
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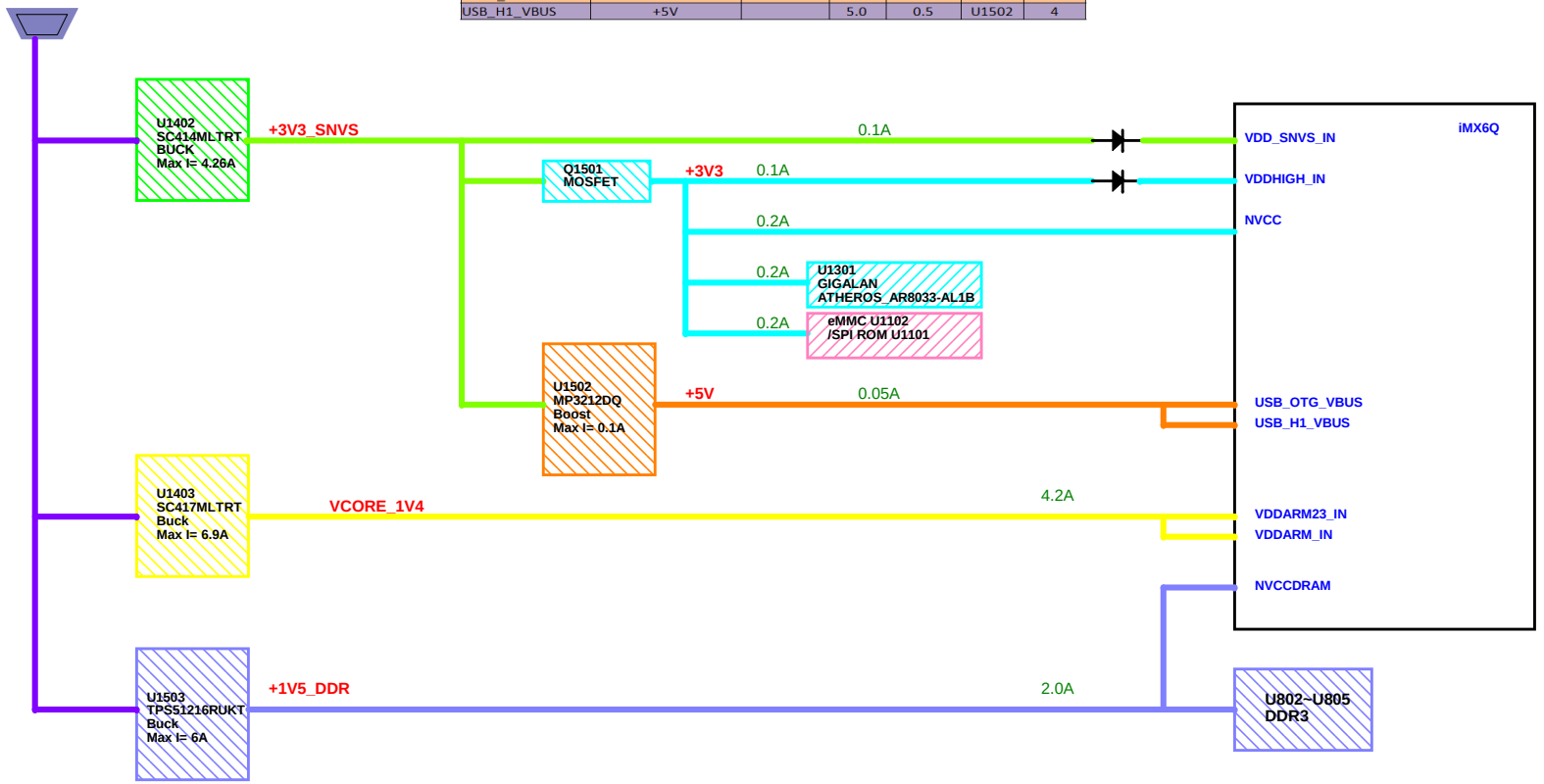
ADVANTECH

Title: System Block Diagram

Size | Document Number: ROM-3420 | Rev: A101-A

Date: Friday, April 18, 2014 | Sheet 2 of 19

Voltage Rail	Rail Name	Supply Reg	Voltage (V)	Max Current (A)	Generated By	Power up sequence
VDD_SNVS_IN	+3V3_SNVS		3.0	200uA	U1501	0
VDDARM_IN VDDARM23_IN	VCORE_1V2		1.2	2.5	U1401	1
VDDSOC_IN	VCORE_1V2		1.2	1.7	U1401	1
VDD_CACHE_CAP*	VDD_1V1_SOC	VDD_SOC_CAP*	1.1		i.MX	1*
VDDHIGH_IN	+3V3		3.0	2.0	U1501	2
NVCC_RGMII NVCC_DRAM	+1V5_DDR		1.5	2.5	U1402	3
DRAM_VREF	DDR_REF		0.75	0.01	U1402	3
NVCC_CSI NVCC_EIM0, 1, 2 NVCC_ENET NVCC_GPIO NVCC_LCD NVCC_NANDF NVCC_SD1, 2 NVCC_SD3 NVCC_JTAG	+3V3		3.3	3.0 System Dependent	U1501	3
USB_H1_VBUS	+5V		5.0	0.5	U1502	4

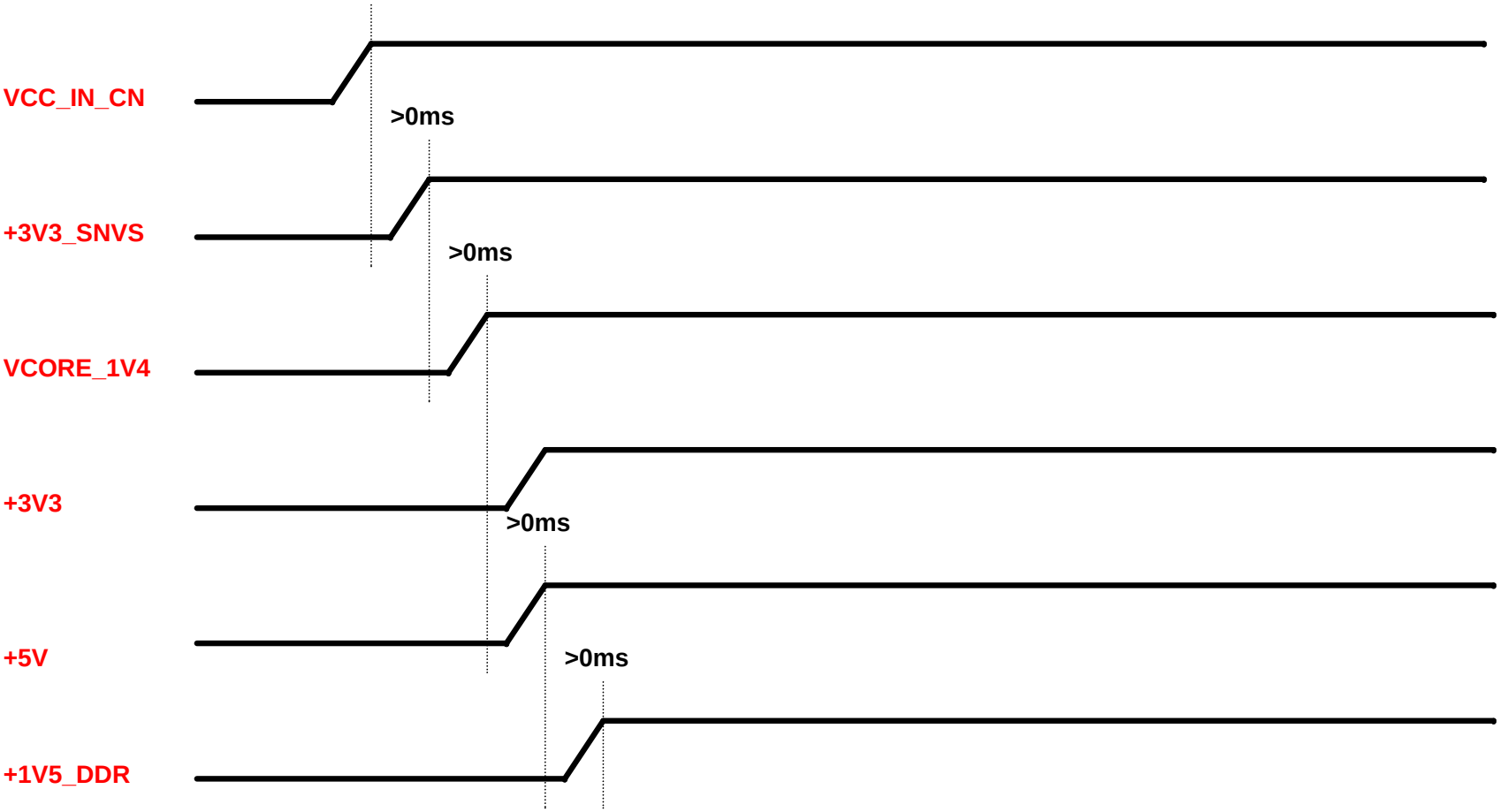


ADVANTECH

Title: Power Block Diagram

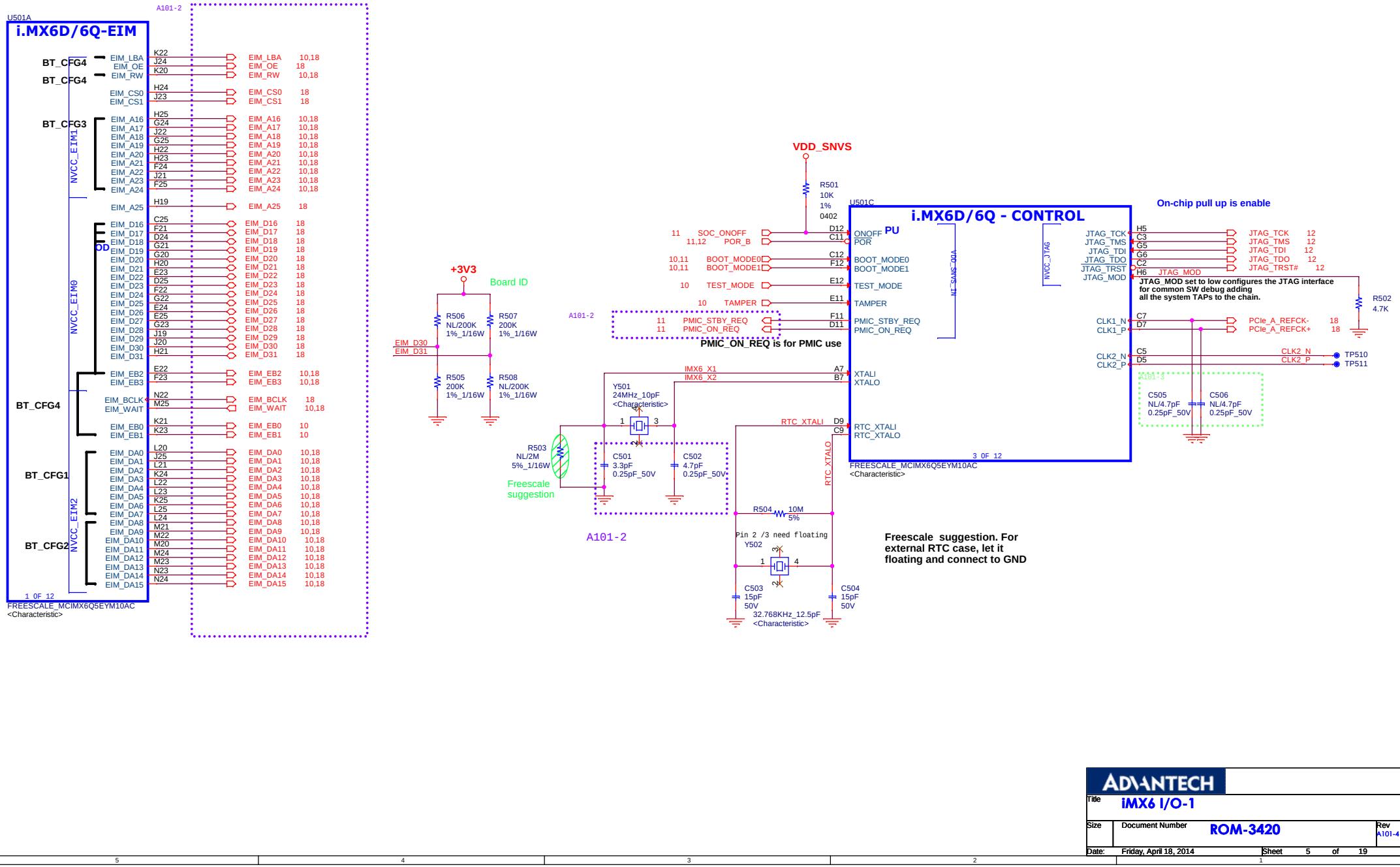
Size | Document Number: ROM-3420 | Rev: A101-4

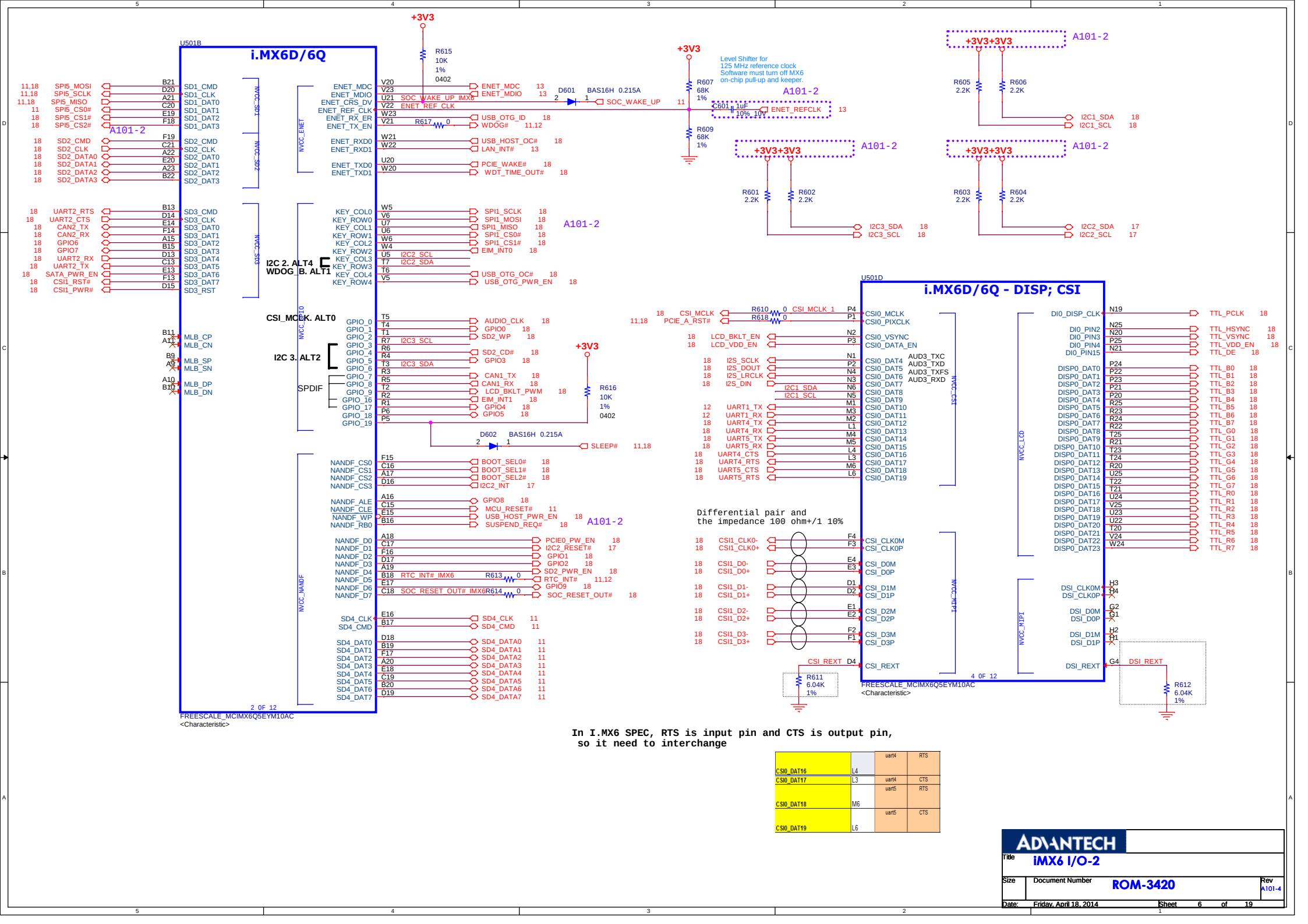
Date: Friday, April 18, 2014 | Sheet 3 of 19

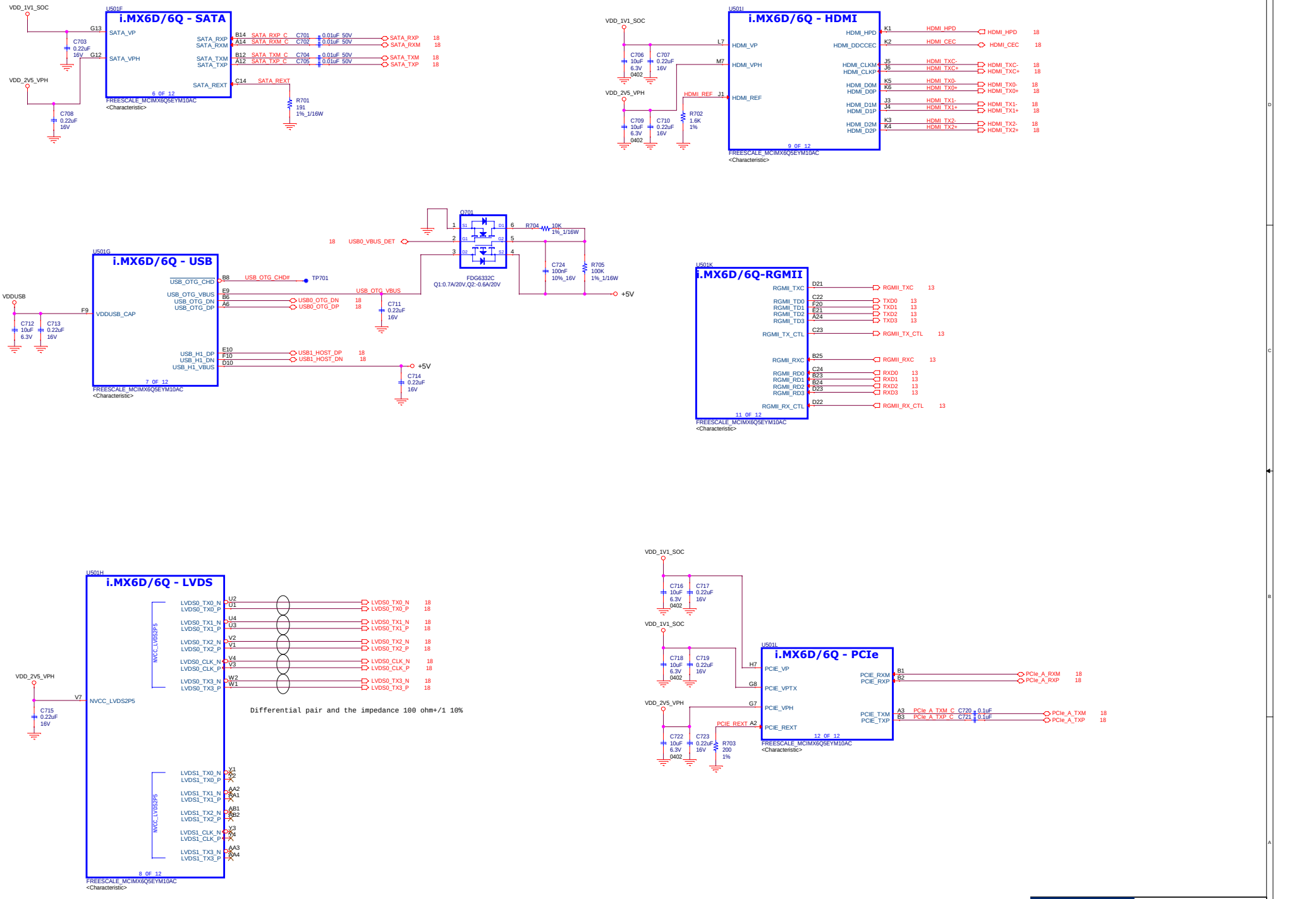


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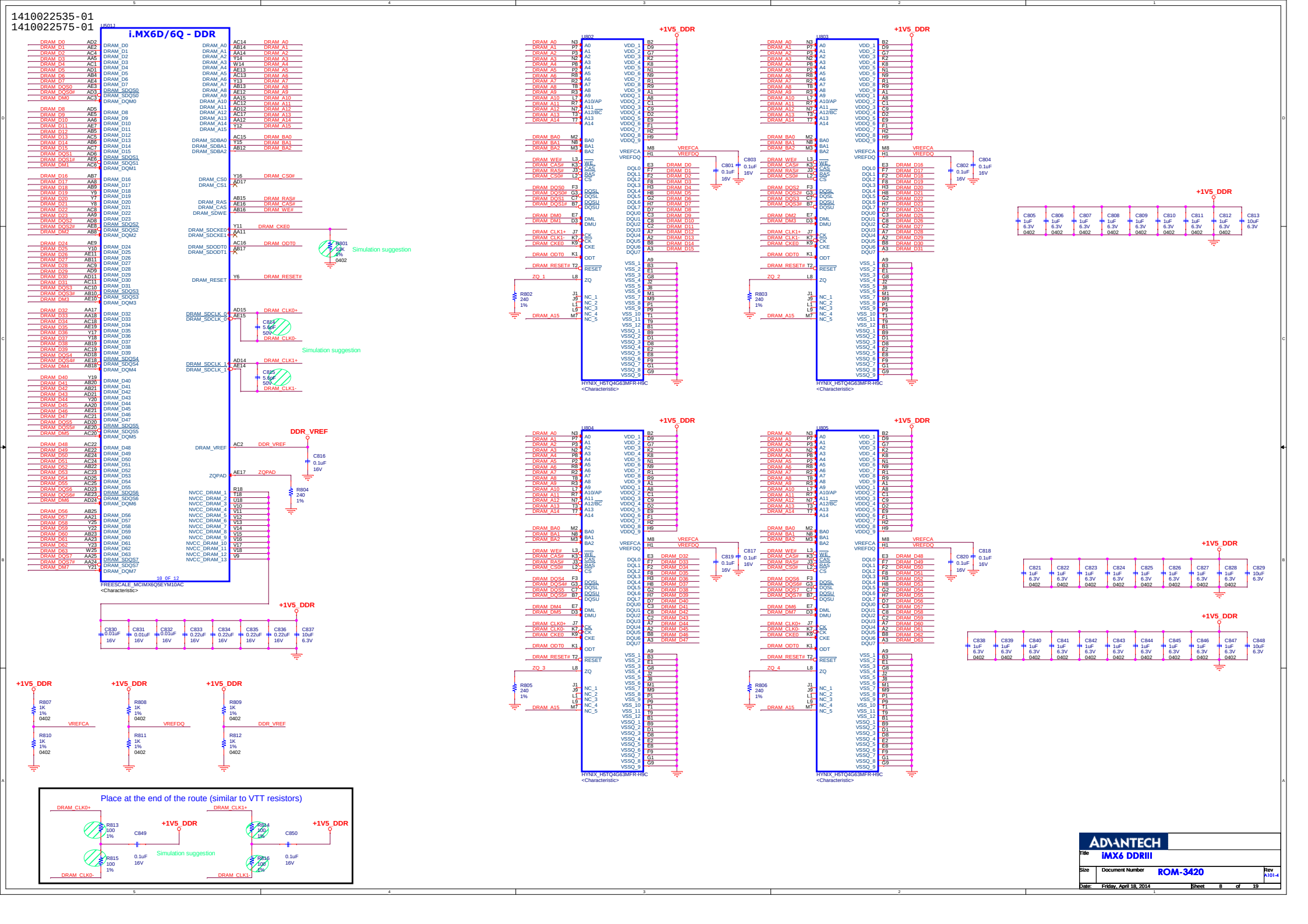
Title	Power Enable Sequence		
Size	Document Number ROM-3420		Rev A101-4
Date: Friday, April 18, 2014		Sheet 4 of 19	

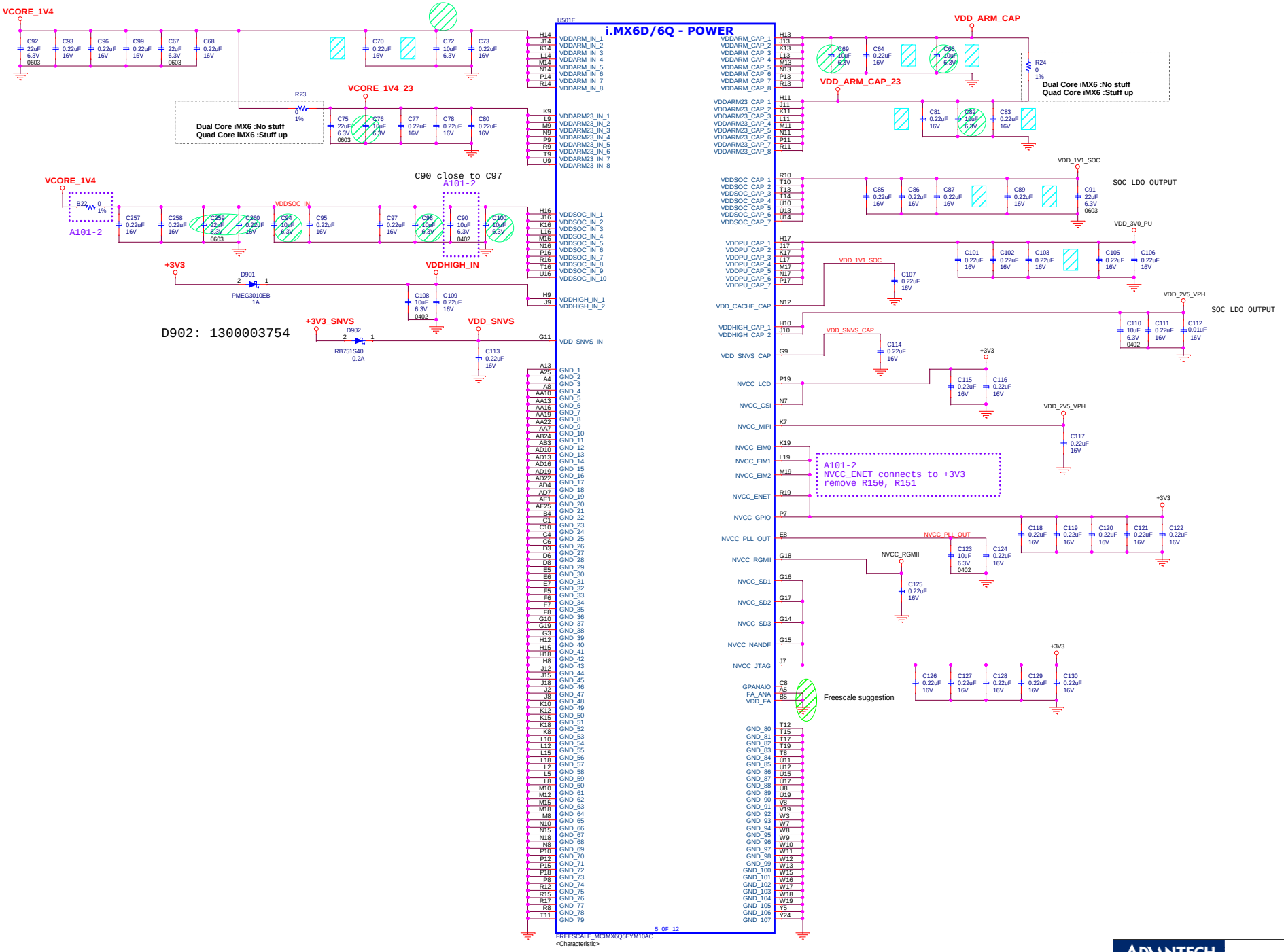

U501A
i.MX6D/6Q-EIM
A101-2
BT_CFG4
BT_CFG4
BT_CFG3
BT_CFG4
BT_CFG1
BT_CFG2
NVCC_EIM1
NVCC_EIM0
NVCC_EIM2
OD
EIM_LBA K22 EIM_LBA 10,18
EIM_OE J24 EIM_OE 18
EIM_RW K20 EIM_RW 10,18
EIM_CS0 H24 EIM_CS0 18
EIM_CS1 J23 EIM_CS1 18
EIM_A16 H25 EIM_A16 10,18
EIM_A17 G24 EIM_A17 10,18
EIM_A18 J22 EIM_A18 10,18
EIM_A19 G25 EIM_A19 10,18
EIM_A20 H22 EIM_A20 10,18
EIM_A21 H23 EIM_A21 10,18
EIM_A22 F24 EIM_A22 10,18
EIM_A23 J21 EIM_A23 10,18
EIM_A24 F25 EIM_A24 10,18
EIM_A25 H19 EIM_A25 18
EIM_D16 C25 EIM_D16 18
EIM_D17 F21 EIM_D17 18
EIM_D18 D24 EIM_D18 18
EIM_D19 G21 EIM_D19 18
EIM_D20 G20 EIM_D20 18
EIM_D21 H20 EIM_D21 18
EIM_D22 E23 EIM_D22 18
EIM_D23 D25 EIM_D23 18
EIM_D24 F22 EIM_D24 18
EIM_D25 G22 EIM_D25 18
EIM_D26 E24 EIM_D26 18
EIM_D27 E25 EIM_D27 18
EIM_D28 G23 EIM_D28 18
EIM_D29 J19 EIM_D29 18
EIM_D30 J20 EIM_D30 18
EIM_D31 H21 EIM_D31 18
EIM_EB2 E22 EIM_EB2 10,18
EIM_EB3 F23 EIM_EB3 10,18
EIM_BCLK N22 EIM_BCLK 18
EIM_WAIT M25 EIM_WAIT 10,18
EIM_EB0 K21 EIM_EB0 10
EIM_EB1 K23 EIM_EB1 10
EIM_DA0 L20 EIM_DA0 10,18
EIM_DA1 J25 EIM_DA1 10,18
EIM_DA2 L21 EIM_DA2 10,18
EIM_DA3 K24 EIM_DA3 10,18
EIM_DA4 L22 EIM_DA4 10,18
EIM_DA5 L23 EIM_DA5 10,18
EIM_DA6 K25 EIM_DA6 10,18
EIM_DA7 L25 EIM_DA7 10,18
EIM_DA8 L24 EIM_DA8 10,18
EIM_DA9 M21 EIM_DA9 10,18
EIM_DA10 M22 EIM_DA10 10,18
EIM_DA11 M20 EIM_DA11 10,18
EIM_DA12 M24 EIM_DA12 10,18
EIM_DA13 M23 EIM_DA13 10,18
EIM_DA14 N23 EIM_DA14 10,18
EIM_DA15 N24 EIM_DA15 10,18
1 OF 12
FREESCALE_MCIMX6Q5EYM10AC
<Characteristic>
VDD_SNVS
R501
10K
1%
0402
U501C
i.MX6D/6Q - CONTROL
ONOFF PU
POR
BOOT_MODE0
BOOT_MODE1
TEST_MODE
TAMPER
PMIC_STBY_REQ
PMIC_ON_REQ
XTALI
XTALO
RTC_XTALI
RTC_XTALO
NT_SANS_100A
NVCC_JTAG
3 OF 12
FREESCALE_MCIMX6Q5EYM10AC
<Characteristic>
11 SOC_ONOFF
11,12 POR_B
10,11 BOOT_MODE0
10,11 BOOT_MODE1
10 TEST_MODE
10 TAMPER
11 PMIC_STBY_REQ
11 PMIC_ON_REQ
PMIC_ON_REQ is for PMIC use
+3V3
Board ID
R506 NL/200K 1%_1/16W
R507 200K 1%_1/16W
R505 200K 1%_1/16W
R508 NL/200K 1%_1/16W
EIM_D30
EIM_D31
IMX6_X1
IMX6_X2
Y501
24MHz_10pF
<Characteristic>
R503
NL/2M
5%_1/16W
Freescale suggestion
C501 3.3pF 0.25pF_50V
C502 4.7pF 0.25pF_50V
R504 10M 5%
Pin 2 /3 need floating
Y502
C503 15pF 50V
C504 15pF 50V
32.768KHz_12.5pF
<Characteristic>
A101-2
Freescale suggestion. For external RTC case, let it floating and connect to GND
On-chip pull up is enable
JTAG_TCK H5 JTAG_TCK 12
JTAG_TMS C3 JTAG_TMS 12
JTAG_TDI G5 JTAG_TDI 12
JTAG_TDO G6 JTAG_TDO 12
JTAG_TRST C2 JTAG_TRST# 12
JTAG_MOD H6 JTAG_MOD
JTAG_MOD set to low configures the JTAG interface for common SW debug adding all the system TAPs to the chain.
R502 4.7K
CLK1_N C7 PCIe_A_REFCK- 18
CLK1_P D7 PCIe_A_REFCK+ 18
CLK2_N C5 CLK2_N TP510
CLK2_P D5 CLK2_P TP511
C505 NL/4.7pF 0.25pF_50V
C506 NL/4.7pF 0.25pF_50V
ADVANTECH
Title iMX6 I/O-1
Size
Document Number ROM-3420
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Date: Friday, April 18, 2014
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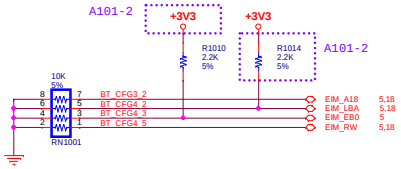

U501B
i.MX6D/6Q
+3V3
R615
10K
1%
0402
SPI5_MOSI
SPI5_SCLK
SPI5_MISO
SPI5_CS0#
SPI5_CS1#
SPI5_CS2#
A101-2
SD2_CMD
SD2_CLK
SD2_DATA0
SD2_DATA1
SD2_DATA2
SD2_DATA3
UART2_RTS
UART2_CTS
CAN2_TX
CAN2_RX
GPIO6
GPIO7
UART2_RX
UART2_TX
SATA_PWR_EN
CSI1_RST#
CSI1_PWR#
I2C 2. ALT4
WDOG_B. ALT1
CSI_MCLK. ALT0
I2C 3. ALT2
SPDIF
MLB_CP
MLB_CN
MLB_SP
MLB_SN
MLB_DP
MLB_DN
ENET_MDC
ENET_MDIO
ENET_CRS_DV
ENET_REF_CLK
ENET_RX_ER
ENET_TX_EN
ENET_RXD0
ENET_RXD1
ENET_TXD0
ENET_TXD1
SOC_WAKE_UP_IMX6
ENET_REF_CLK
R617 0
USB_OTG_ID
WDOG#
USB_HOST_OC#
LAN_INT#
PCIE_WAKE#
WDT_TIME_OUT#
D601 BAS16H 0.215A
SOC_WAKE_UP
Level Shifter for
125 MHz reference clock
Software must turn off MX6
on-chip pull-up and keeper.
R607
68K
1%
R609
68K
1%
C601 1uF
10% 10V
ENET_REFCLK
+3V3+3V3
R605 2.2K
R606 2.2K
I2C1_SDA
I2C1_SCL
R601 2.2K
R602 2.2K
I2C3_SDA
I2C3_SCL
R603 2.2K
R604 2.2K
I2C2_SDA
I2C2_SCL
KEY_COL0
KEY_ROW0
KEY_COL1
KEY_ROW1
KEY_COL2
KEY_ROW2
KEY_COL3
KEY_ROW3
KEY_COL4
KEY_ROW4
SPI1_SCLK
SPI1_MOSI
SPI1_MISO
SPI1_CS0#
SPI1_CS1#
EIM_INT0
USB_OTG_OC#
USB_OTG_PWR_EN
I2C2_SCL
I2C2_SDA
GPIO_0
GPIO_1
GPIO_2
GPIO_3
GPIO_4
GPIO_5
GPIO_6
GPIO_7
GPIO_8
GPIO_9
GPIO_16
GPIO_17
GPIO_18
GPIO_19
AUDIO_CLK
GPIO0
SD2_WP
SD2_CD#
GPIO3
CAN1_TX
CAN1_RX
LCD_BKLT_PWM
EIM_INT1
GPIO4
GPIO5
R616
10K
1%
0402
D602 BAS16H 0.215A
SLEEP#
NANDF_CS0
NANDF_CS1
NANDF_CS2
NANDF_CS3
NANDF_ALE
NANDF_CLE
NANDF_WP
NANDF_RB0
NANDF_D0
NANDF_D1
NANDF_D2
NANDF_D3
NANDF_D4
NANDF_D5
NANDF_D6
NANDF_D7
BOOT_SEL0#
BOOT_SEL1#
BOOT_SEL2#
I2C2_INT
GPIO8
MCU_RESET#
USB_HOST_PWR_EN
SUSPEND_REQ#
PCIE0_PW_EN
I2C2_RESET#
GPIO1
GPIO2
SD2_PWR_EN
RTC_INT#
GPIO9
SOC_RESET_OUT#
RTC_INT# IMX6
SOC_RESET_OUT# IMX6
R613 0
R614 0
SD4_CLK
SD4_CMD
SD4_DATA0
SD4_DATA1
SD4_DATA2
SD4_DATA3
SD4_DATA4
SD4_DATA5
SD4_DATA6
SD4_DATA7
2 OF 12
FREESCALE_MCIMX6Q5EYM10AC
<Characteristic>
U501D
i.MX6D/6Q - DISP; CSI
CSI_MCLK
PCIE_A_RST#
R610 0 CSI_MCLK_1
R618 0
CSI0_MCLK
CSI0_PIXCLK
CSI0_VSYNC
CSI0_DATA_EN
LCD_BKLT_EN
LCD_VDD_EN
I2S_SCLK
I2S_DOUT
I2S_LRCLK
I2S_DIN
CSI0_DAT4
CSI0_DAT5
CSI0_DAT6
CSI0_DAT7
CSI0_DAT8
CSI0_DAT9
CSI0_DAT10
CSI0_DAT11
CSI0_DAT12
CSI0_DAT13
CSI0_DAT14
CSI0_DAT15
CSI0_DAT16
CSI0_DAT17
CSI0_DAT18
CSI0_DAT19
AUD3_TXC
AUD3_TXD
AUD3_TXFS
AUD3_RXD
UART1_TX
UART1_RX
UART4_TX
UART4_RX
UART5_TX
UART5_RX
UART4_CTS
UART4_RTS
UART5_CTS
UART5_RTS
Differential pair and
the impedance 100 ohm+/1 10%
CSI1_CLK0-
CSI1_CLK0+
CSI1_D0-
CSI1_D0+
CSI1_D1-
CSI1_D1+
CSI1_D2-
CSI1_D2+
CSI1_D3-
CSI1_D3+
CSI_CLK0M
CSI_CLK0P
CSI_D0M
CSI_D0P
CSI_D1M
CSI_D1P
CSI_D2M
CSI_D2P
CSI_D3M
CSI_D3P
CSI_REXT
R611
6.04K
1%
4 OF 12
FREESCALE_MCIMX6Q5EYM10AC
<Characteristic>
DI0_DISP_CLK
DI0_PIN2
DI0_PIN3
DI0_PIN4
DI0_PIN15
DISP0_DAT0
DISP0_DAT1
DISP0_DAT2
DISP0_DAT3
DISP0_DAT4
DISP0_DAT5
DISP0_DAT6
DISP0_DAT7
DISP0_DAT8
DISP0_DAT9
DISP0_DAT10
DISP0_DAT11
DISP0_DAT12
DISP0_DAT13
DISP0_DAT14
DISP0_DAT15
DISP0_DAT16
DISP0_DAT17
DISP0_DAT18
DISP0_DAT19
DISP0_DAT20
DISP0_DAT21
DISP0_DAT22
DISP0_DAT23
TTL_PCLK
TTL_HSYNC
TTL_VSYNC
TTL_VDD_EN
TTL_DE
TTL_B0
TTL_B1
TTL_B2
TTL_B3
TTL_B4
TTL_B5
TTL_B6
TTL_B7
TTL_G0
TTL_G1
TTL_G2
TTL_G3
TTL_G4
TTL_G5
TTL_G6
TTL_G7
TTL_R0
TTL_R1
TTL_R2
TTL_R3
TTL_R4
TTL_R5
TTL_R6
TTL_R7
DSI_CLK0M
DSI_CLK0P
DSI_D0M
DSI_D0P
DSI_D1M
DSI_D1P
DSI_REXT
R612
6.04K
1%
In I.MX6 SPEC, RTS is input pin and CTS is output pin,
so it need to interchange
CSI0_DAT16 L4 uart4 RTS
CSI0_DAT17 L3 uart4 CTS
CSI0_DAT18 M6 uart5 RTS
CSI0_DAT19 L6 uart5 CTS
ADVANTECH
Title
iMX6 I/O-2
Size
Document Number
ROM-3420
Rev
A101-4
Date: Friday, April 18, 2014
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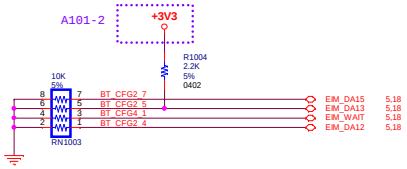

U501F
i.MX6D/6Q - SATA
VDD_1V1_SOC
VDD_2V5_VPH
SATA_VP
SATA_VPH
SATA_RXP
SATA_RXM
SATA_TXM
SATA_TXP
SATA_REXT
SATA_RXP_C
SATA_RXM_C
SATA_TXM_C
SATA_TXP_C
C703 0.22uF 16V
C708 0.22uF 16V
C701 0.01uF 50V
C702 0.01uF 50V
C704 0.01uF 50V
C705 0.01uF 50V
C14 SATA_REXT
R701 191 1%_1/16W
6 OF 12
FREESCALE_MCIMX6Q5EYM10AC
<Characteristic>
U501I
i.MX6D/6Q - HDMI
HDMI_VP
HDMI_VPH
HDMI_REF
HDMI_HPD
HDMI_DDCCEC
HDMI_CLKM
HDMI_CLKP
HDMI_D0M
HDMI_D0P
HDMI_D1M
HDMI_D1P
HDMI_D2M
HDMI_D2P
C706 10uF 6.3V 0402
C707 0.22uF 16V
C709 10uF 6.3V 0402
C710 0.22uF 16V
R702 1.6K 1%
9 OF 12
U501G
i.MX6D/6Q - USB
VDDUSB
VDDUSB_CAP
USB_OTG_CHD
USB_OTG_VBUS
USB_OTG_DN
USB_OTG_DP
USB_H1_DP
USB_H1_DN
USB_H1_VBUS
USB_OTG_CHD#
TP701
USB0_OTG_DN
USB0_OTG_DP
USB1_HOST_DP
USB1_HOST_DN
USB0_VBUS_DET
Q701
FDG6332C
Q1:0.7A/20V,Q2:-0.6A/20V
R704 10K 1%_1/16W
R705 100K 1%_1/16W
C724 100nF 10%_16V
C711 0.22uF 16V
C712 10uF 6.3V
C713 0.22uF 16V
C714 0.22uF 16V
+5V
7 OF 12
U501K
i.MX6D/6Q-RGMII
RGMII_TXC
RGMII_TD0
RGMII_TD1
RGMII_TD2
RGMII_TD3
RGMII_TX_CTL
RGMII_RXC
RGMII_RD0
RGMII_RD1
RGMII_RD2
RGMII_RD3
RGMII_RX_CTL
TXD0
TXD1
TXD2
TXD3
RXD0
RXD1
RXD2
RXD3
11 OF 12
U501H
i.MX6D/6Q - LVDS
NVCC_LVDS2P5
LVDS0_TX0_N
LVDS0_TX0_P
LVDS0_TX1_N
LVDS0_TX1_P
LVDS0_TX2_N
LVDS0_TX2_P
LVDS0_CLK_N
LVDS0_CLK_P
LVDS0_TX3_N
LVDS0_TX3_P
LVDS1_TX0_N
LVDS1_TX0_P
LVDS1_TX1_N
LVDS1_TX1_P
LVDS1_TX2_N
LVDS1_TX2_P
LVDS1_CLK_N
LVDS1_CLK_P
LVDS1_TX3_N
LVDS1_TX3_P
C715 0.22uF 16V
8 OF 12
Differential pair and the impedance 100 ohm+/1 10%
U501L
i.MX6D/6Q - PCIe
PCIE_VP
PCIE_VPTX
PCIE_VPH
PCIE_REXT
PCIE_RXM
PCIE_RXP
PCIE_TXM
PCIE_TXP
PCIE_REXT
PCIe_A_TXM_C
PCIe_A_TXP_C
C716 10uF 6.3V 0402
C717 0.22uF 16V
C718 10uF 6.3V 0402
C719 0.22uF 16V
C720 0.1uF
C721 0.1uF
C722 10uF 6.3V 0402
C723 0.22uF 16V
R703 200 1%
12 OF 12
ADVANTECH
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1410022575-01



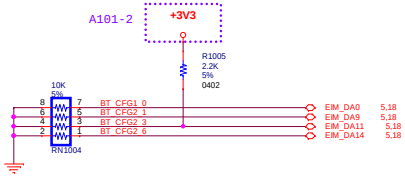

i.MX6D/6Q - POWER
U501E
VCORE_1V4
VCORE_1V4_23
Dual Core iMX6 :No stuff
Quad Core iMX6 :Stuff up
C90 close to C97
A101-2
VDDSOC_IN
+3V3
VDDHIGH_IN
D901
PMEG3010EB
1A
D902: 1300003754
+3V3_SNVS
VDD_SNVS
D902
RB751S40
0.2A
VDD_ARM_CAP
VDD_ARM_CAP_23
VDD_1V1_SOC
SOC LDO OUTPUT
VDD_3V0_PU
VDD_2V5_VPH
VDD_SNVS_CAP
A101-2
NVCC_ENET connects to +3V3
remove R150, R151
NVCC_PLL_OUT
NVCC_RGMII
Freescale suggestion
5 OF 12
FREESCALE_MCIMX6Q5EYM10AC
<Characteristic>
ADVANTECH
Title
iMX6 Power & GND
Size
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ROM-3420
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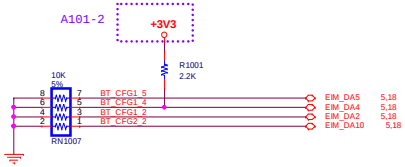






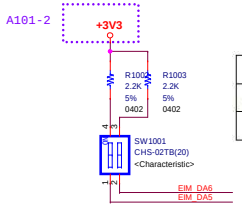




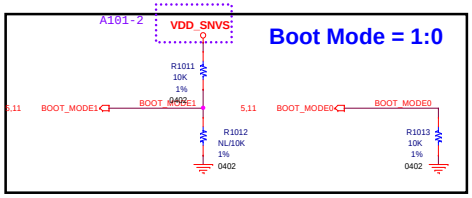


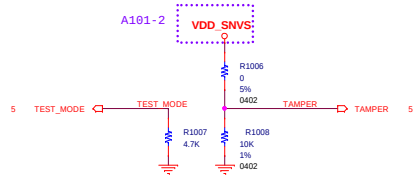
Boot Configuration Select

Default Boot Device = SPI5



	EIM_DA6	EIM_DA5
Serial-ROM	0	1
SD/eSD	1	0





Boot Mode

BOOT_MODE [1]	BOOT_MODE [0]	Boot Type	Boot Details
0	0	Boot from fuses	Like 10, but boot fuses will be always used, if BT_FUSE_SEL=1
0	1	Serial Download via USB	Load and execute code, via serial device: USB (high-speed, non-stream, bulk mode)
1	0	Normal Boot (Development)	Executing ROM code, which handles booting from following sources NOR Flash (via WEIM, 16-bit, slow asynchronous mode for debugging purpose only) OneNAND SPI (serial flash) / I2C NAND Flash SD/MMC /MoviNAND SATA (Hard disk or SSD) A fallback to ALL above modes, on error exception: USB If BT_FUSE_SEL=0, GPIO boot pins will be sampled.
1	1	FSL Test Mode	Freescale Test Mode, special mode reserved for device testing.

BOOT_CFG1[7]	BOOT_CFG1[6]	BOOT_CFG1[5]	BOOT_CFG1[4]	BOOT_CFG1[3]	BOOT_CFG1[2]	BOOT_CFG1[1]	BOOT_CFG1[0]
L1 I-Cache DISABLE	BT_MMU_DISABLE	DDR Memory Map default config '00' - Single DDR channel '01' - Fixed 2x32 map '10' - 4KB Interleaving Enabled '11' - Illegal	Reserved	Boot Frequencies (ARM/DDR) 0 – ARM792/ DDR528 MHz 1 – ARM396/ DDR352 MHz	Reserved	Reserved	Reserved
BOOT_CFG2[7]	BOOT_CFG2[6]	BOOT_CFG2[5]	BOOT_CFG2[4]	BOOT_CFG2[3]	BOOT_CFG2[2]	BOOT_CFG2[1]	BOOT_CFG2[0]
Reserved	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3	SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - eCSPI5 101 - I2C1 110 - I2C2 111 - I2C3			

Reserved configuration switch should be set to '0' (OFF)

SW1

	BOOT_CFG1 [7]	BOOT_CFG1 [6]	BOOT_CFG1 [5]	BOOT_CFG1 [4]	BOOT_CFG1 [3]	BOOT_CFG1 [2]	BOOT_CFG1 [1]	BOOT_CFG1 [0]
Reserved-NVM	0	0	0	1	Reserved	Reserved	Reserved	Reserved
WEIM	0	0	0	0	Memory Type: 0 - NOR Flash 1 - OneNAND	Reserved	Reserved	Reserved
SATA	0	0	1	0	Reserved	Reserved	Reserved	Reserved
Serial-ROM	0	0	1	1	Reserved	Reserved	Reserved	Reserved
SD/eSD	0	1	0	Fast Boot: 0 - Regular 1 - Fast Boot	SD/SDXC Speed 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104		Reserved (SDXC power control - XPC) 100mA/150mA TBD	SD Loopback Clock Source Sel '0' - direct '1' - through SD pad
MMC/eMMC	0	1	1	Fast Boot: 0 - Regular 1 - Fast Boot	SD/MMC Speed 0 - High 1- Normal	Reserved	Reserved	MMC Loopback Clock Source Sel '0' - direct '1' - through SD pad
NAND	1	Reserved (Freq select)	BT_TOGGLEMODE	Override Pad Settings (using PAD_SETTINGS value)	Interleave Scheme: (TBD)		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	

Reserved configuration switch should be set to '0' (OFF)

SW2

	BOOT_CFG2 [7]	BOOT_CFG2 [6]	BOOT_CFG2 [5]	BOOT_CFG2 [4]	BOOT_CFG2 [3]	BOOT_CFG2 [2]	BOOT_CFG2 [1]	BOOT_CFG2 [0]
Reserved-NVM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
WEIM	Muxing Scheme: A/D16 (HW Default in external boot) A+DH A+DL A/D32		OneNand Page Size: 00 - 1KB 01 - 2KB 10 - 4KB 11 - Reserved		Reserved	Reserved	Reserved	Reserved
SATA	Reserved	Reserved	Reserved	Tx Spread Spectrum '0' - Disabled '1' - Enabled	Rx Spread Spectrum '0' - Disabled '1' - Enabled	SATA_SPEED 0 - Gen2 (3.0Gbps) 1 - Gen1 (1.5Gbps)	SATA Type: '00' - I '01' - m '10' - x '11' - Reserved	
Serial-ROM	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
SD/eSD	SD Calibration Step '00' - 1 TBD		Bus Width: 0 - 1-bit 1 - 4-bit	Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3 11 - eSDHC4		Reserved (SDXC Current Limit) 200mA/400mA/600mA/800mA (TBD)		Override Pad Settings (using PAD_SETTINGS value)
MMC/eMMC	Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Port Select: 00 - eSDHC1 01 - eSDHC2 10 - eSDHC3 (eMMC4.4) 11 - eSDHC4		DLL Override: 0 - Boot ROM default. 1 - Apply value per fuse field MMC_DLL_DLY[3:0]	Fast Boot Acknowledge Disable: 0 - Boot Ack Enabled 1 - Boot Ack Disabled	Override Pad Settings (using PAD_SETTINGS value)
NAND	Toggle Mode 33MHz Preamble Delay, Read Latency			BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Pages In Block: 00 - 128 01 - 64 10 - 32 11 - Reserved		TBD (LBA-Nand) 0 - Non LBA (11ms delay) 1 - LBA (22ms delay)

Reserved configuration switch should be set to '0' (OFF)

SW3

	BOOT_CFG3 [7]	BOOT_CFG3 [6]	BOOT_CFG3 [5]	BOOT_CFG3 [4]	BOOT_CFG3 [3]	BOOT_CFG3 [2]	BOOT_CFG3 [1]	BOOT_CFG3 [0]
	L1 I-Cache DISABLE	BT_MMU_DISABLE	DDR Memory Map default config '00' - Single DDR channel '01' - Fixed 2x32 map '10' - 4KB Interleaving Enabled '11' - Illegal		Reserved (DDR3 SPI config) '1' - DDR3 config. Read via SPI.	Boot Frequencies (ARM/DDR) 0 - 792 / 528 MHz 1 - 528 / 352MHz	Reserved	Reserved

Reserved configuration switch should be set to '0' (OFF)

SW4

	BOOT_CFG4 [7]	BOOT_CFG4 [6]	BOOT_CFG4 [5]	BOOT_CFG4 [4]	BOOT_CFG4 [3]	BOOT_CFG4 [2]	BOOT_CFG3 [1]	BOOT_CFG3 [0]
	Infinit-Loop (Debug USE only) 0 - Disable 1- Enable	EEPROM Recovery Enable '0' - Disabled '1' - Enabled	CS select (SPI only): 00 - CS#0 (default) 01 - CS#1 10 - CS#2 11 - CS#3		SPI Addressing: 0 - 2-bytes (16-bit) 1 - 3-bytes (24-bit)	Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3 011 - eCSPI4 100 - eCSPI5 101 - I2C1 110 - I2C2 111 - I2C3		

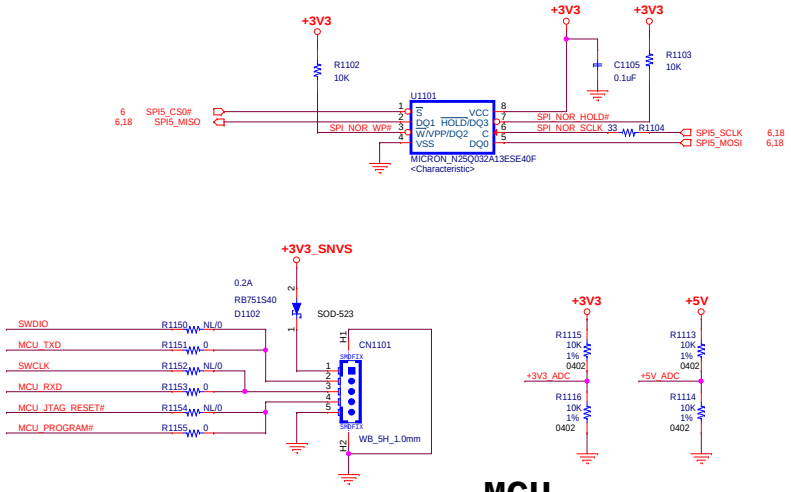
ADVANTECH

Title: iMX6 Strap / IO MUX Table

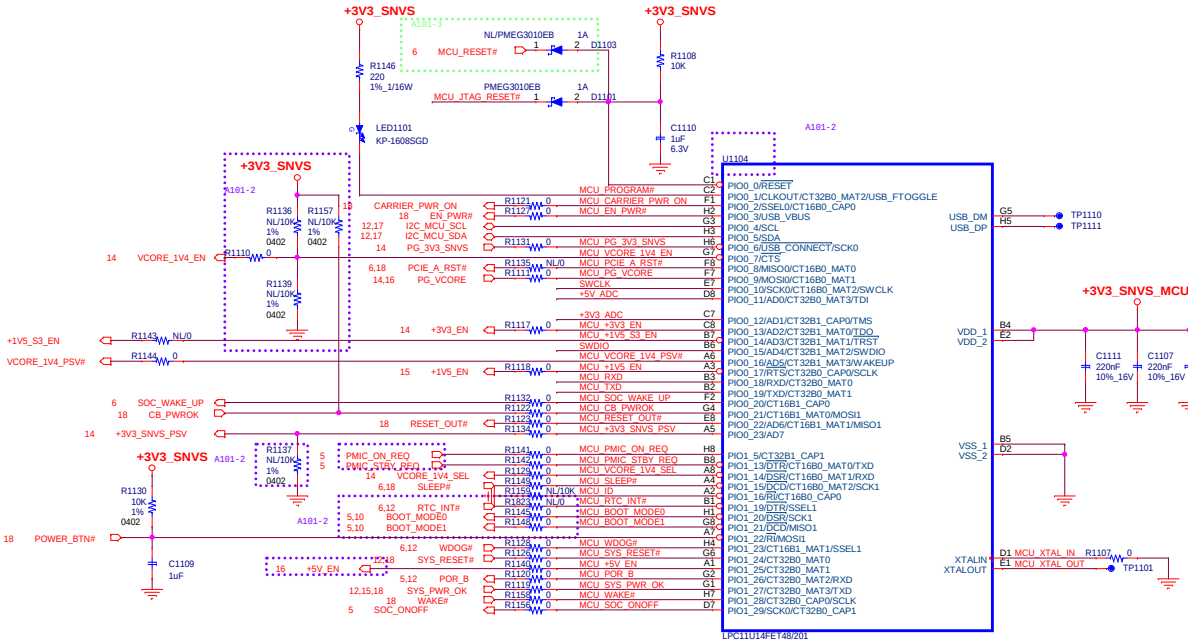
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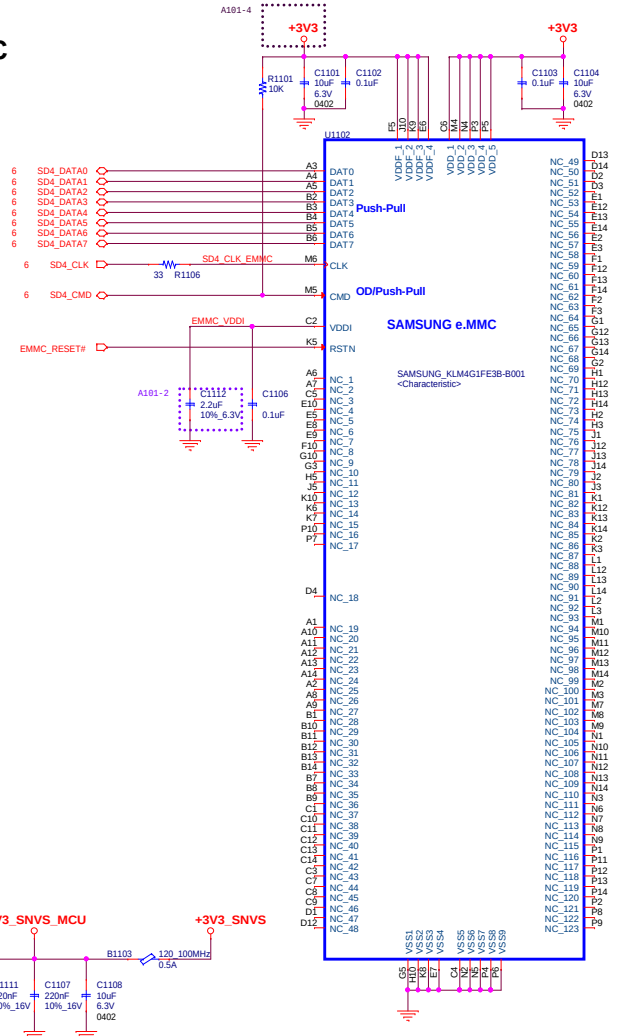
SPI ROM

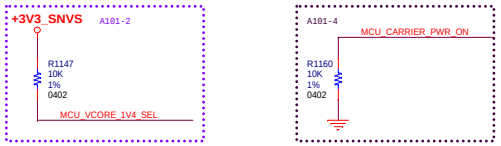


MCU



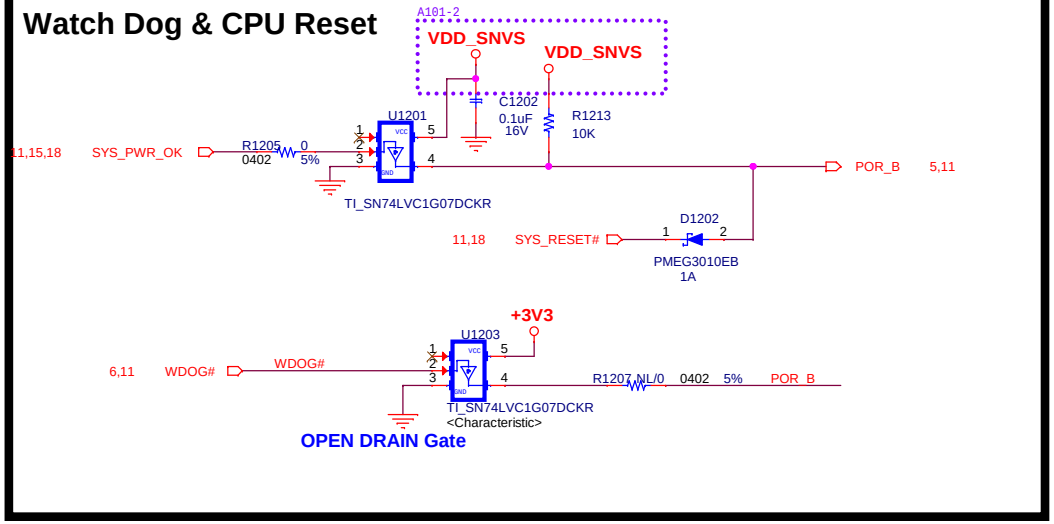
EMMC



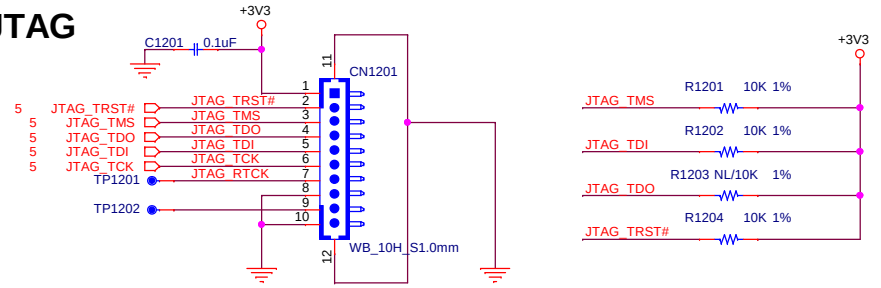


Title	11-eMMC / SPI ROM / MCU
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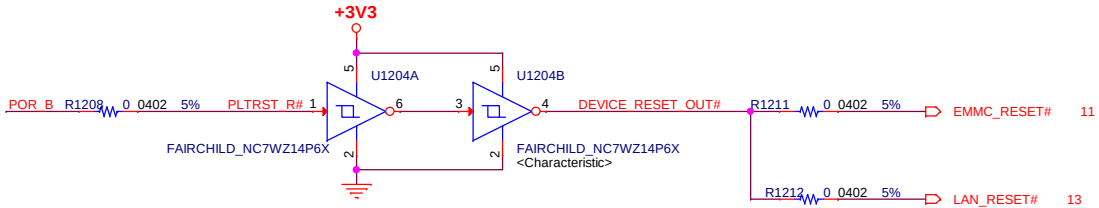
Watch Dog & CPU Reset



JTAG

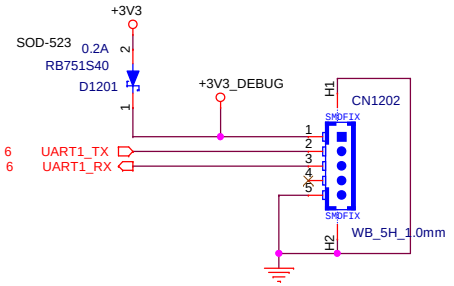


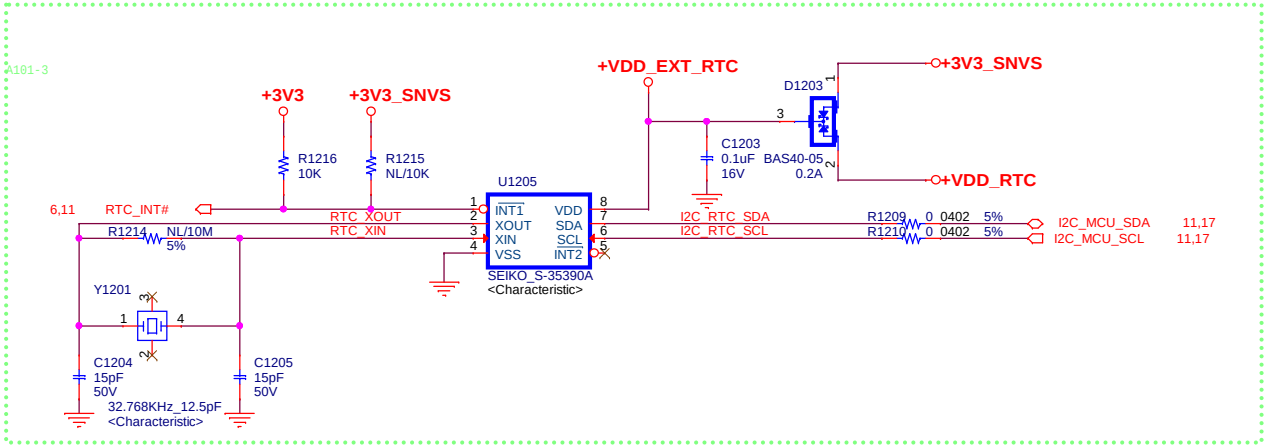
I/O Device Reset



DEBUG Port

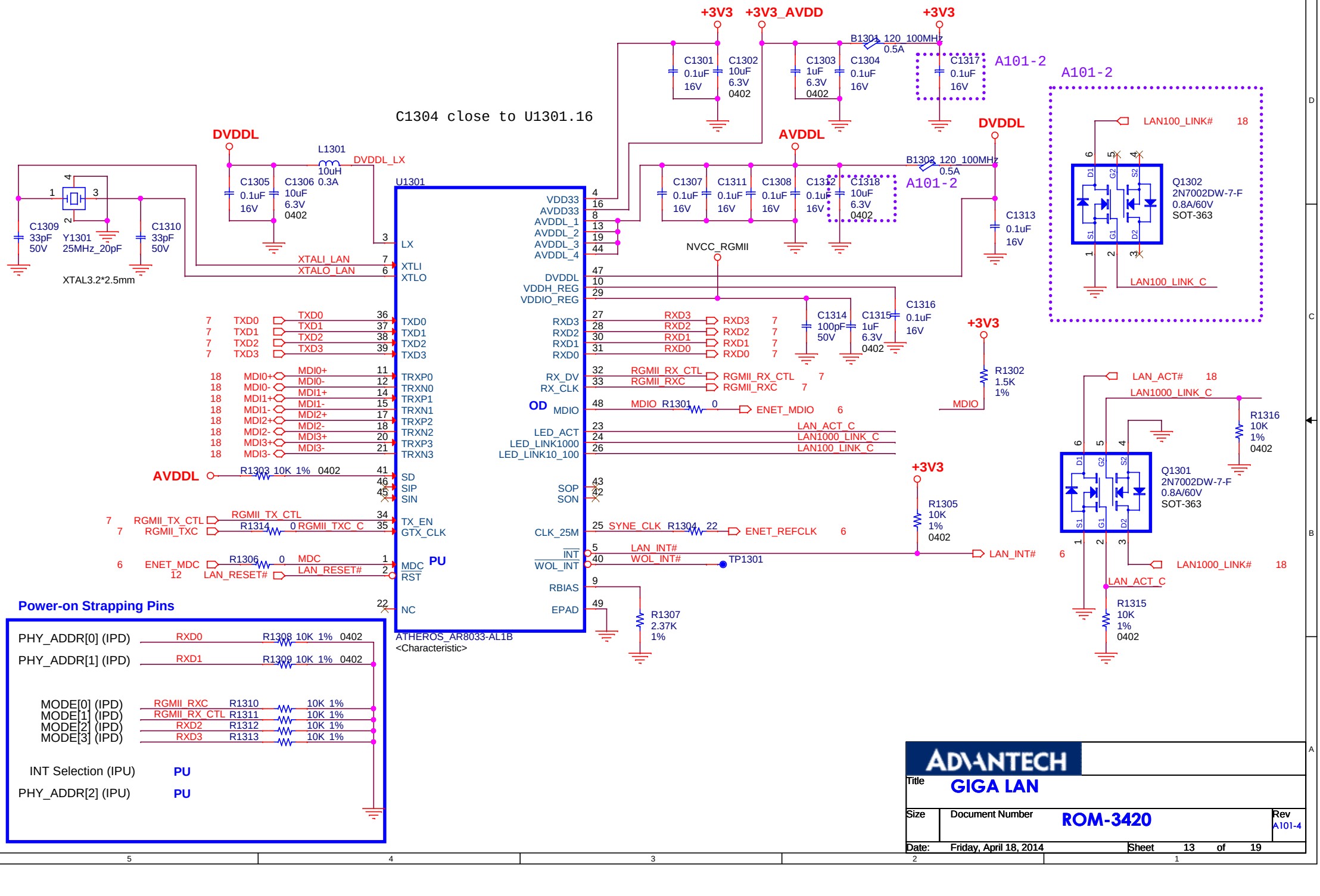
DEBUG port com from UART1





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Title	JTAG/DEBUG PORT/RESET/RTC	
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C1304 close to U1301.16
+3V3
+3V3_AVDD
+3V3
B1301 120_100MHz 0.5A
C1301 0.1uF 16V
C1302 10uF 6.3V 0402
C1303 1uF 6.3V 0402
C1304 0.1uF 16V
C1317 0.1uF 16V
A101-2
A101-2
DVDDL
AVDDL
DVDDL
L1301
10uH
DVDDL_LX
C1305 0.1uF 16V
C1306 0.3A 10uF 6.3V 0402
U1301
B1302 120_100MHz 0.5A
A101-2
C1307 0.1uF 16V
C1311 0.1uF 16V
C1308 0.1uF 16V
C1312 0.1uF 16V
C1318 10uF 6.3V 0402
C1313 0.1uF 16V
LAN100_LINK# 18
Q1302 2N7002DW-7-F 0.8A/60V SOT-363
LAN100_LINK_C
C1309 33pF 50V
Y1301 25MHz_20pF
C1310 33pF 50V
XTAL3.2*2.5mm
XTALI_LAN
XTALO_LAN
LX
XTLI
XTLO
VDD33
AVDD33
AVDDL_1
AVDDL_2
AVDDL_3
AVDDL_4
DVDDL
VDDH_REG
VDDIO_REG
NVCC_RGMII
C1314 100pF 50V
C1315 1uF 6.3V 0402
C1316 0.1uF 16V
+3V3
R1302 1.5K 1%
MDIO
TXD0
TXD1
TXD2
TXD3
TXD0
TXD1
TXD2
TXD3
RXD3
RXD2
RXD1
RXD0
RXD3
RXD2
RXD1
RXD0
MDI0+
MDI0-
MDI1+
MDI1-
MDI2+
MDI2-
MDI3+
MDI3-
TRXP0
TRXN0
TRXP1
TRXN1
TRXP2
TRXN2
TRXP3
TRXN3
RX_DV
RX_CLK
RGMII_RX_CTL
RGMII_RXC
RGMII_RX_CTL
RGMII_RXC
OD
MDIO
MDIO R1301 0
ENET_MDIO
LED_ACT
LED_LINK1000
LED_LINK10_100
LAN_ACT_C
LAN1000_LINK_C
LAN100_LINK_C
LAN_ACT# 18
LAN1000_LINK_C
R1316 10K 1% 0402
Q1301 2N7002DW-7-F 0.8A/60V SOT-363
AVDDL
R1303 10K 1% 0402
SD
SIP
SIN
SOP
SON
+3V3
R1305 10K 1% 0402
RGMII_TX_CTL
RGMII_TXC
R1314 0
RGMII_TXC_C
TX_EN
GTX_CLK
CLK_25M
SYNE_CLK R1304 22
ENET_REFCLK
ENET_MDC
LAN_RESET#
R1306 0
MDC
LAN_RESET#
MDC
RST
PU
INT
WOL_INT
LAN_INT#
WOL_INT#
TP1301
LAN_INT#
LAN1000_LINK# 18
LAN_ACT_C
R1315 10K 1% 0402
RBIAS
EPAD
R1307 2.37K 1%
NC
ATHEROS_AR8033-AL1B
<Characteristic>
Power-on Strapping Pins
PHY_ADDR[0] (IPD)
RXD0
R1308 10K 1% 0402
PHY_ADDR[1] (IPD)
RXD1
R1309 10K 1% 0402
MODE[0] (IPD)
MODE[1] (IPD)
MODE[2] (IPD)
MODE[3] (IPD)
RGMII_RXC
RGMII_RX_CTL
RXD2
RXD3
R1310
R1311
R1312
R1313
10K 1%
INT Selection (IPU)
PU
PHY_ADDR[2] (IPU)
PU
ADVANTECH
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SYS_3V3

SC414
H--> PSV
F--> Continous
G--> Disable

+V5LDO_3V3 +V5LDO_3V3 +V5LDO_3V3 +V5LDO_3V3 +V5LDO_3V3

A101-2

+3V3_SNVS_PSV
H--> PSV
L--> NORMAL

VFB=750mV

SEMTECH_SC414MLTRT
MLPQ28

VFB=750mV

+3V3 @ 2A

Current limit to 3.3A.

Vout=VFB*(1+R1404/R1407)
=0.75*(1+34K/10K)
=3.3V
Ilim=R1405/1090
=3.6K/1090
=3.3A

VCC_IN_CN
1.5A/60mils

VCORE_1V4

Change to OD gate SC417
H--> PSV
F--> Continous
G--> Disable

VCORE_1V4_PSV#
L--> PSV
H--> NORMAL

Disable LDO

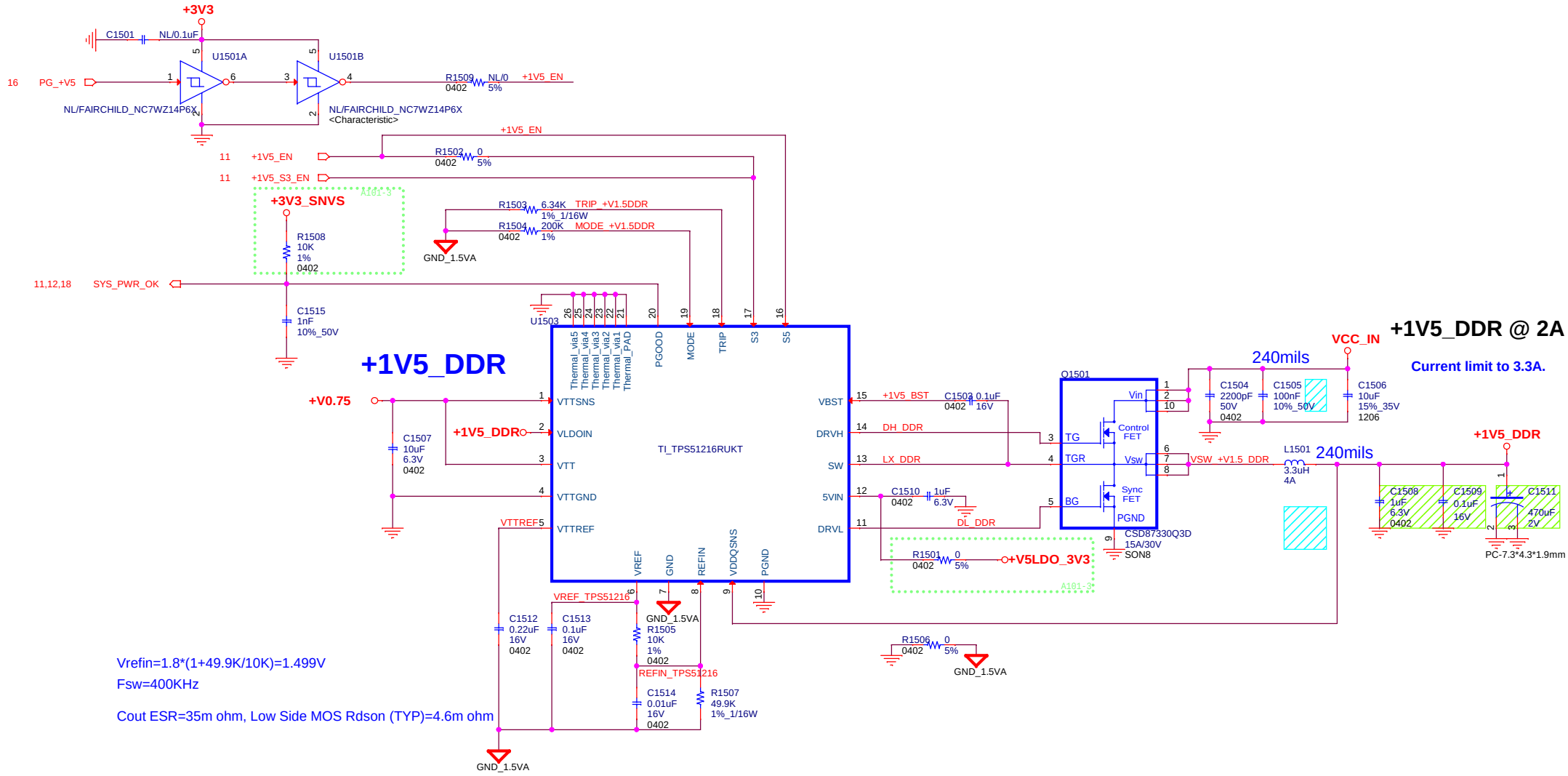
VCORE_1V4@ 4.5A

Vout=VFB*(1+R1418/R1423)
=0.5*(1+39.2K/22K)
=1.391V
Ilim=R1420/735
=5.1K/735
=6.93A

LED Idicator

3V3 Put High Source

Title	DC_IN & VCORE_1V4 & +3V3		
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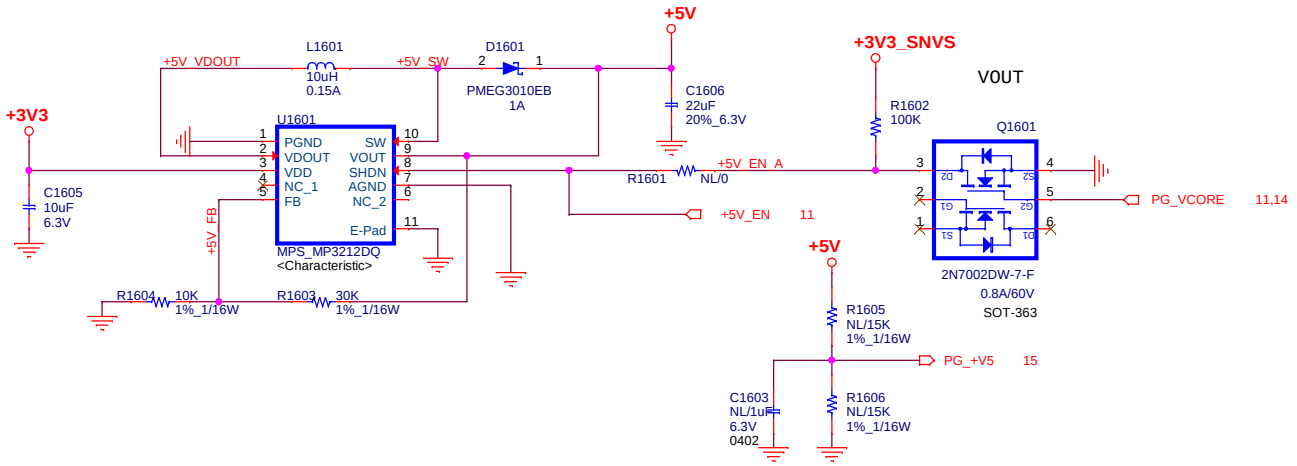


ADVANTECH			
Title	+1V5_DDR		
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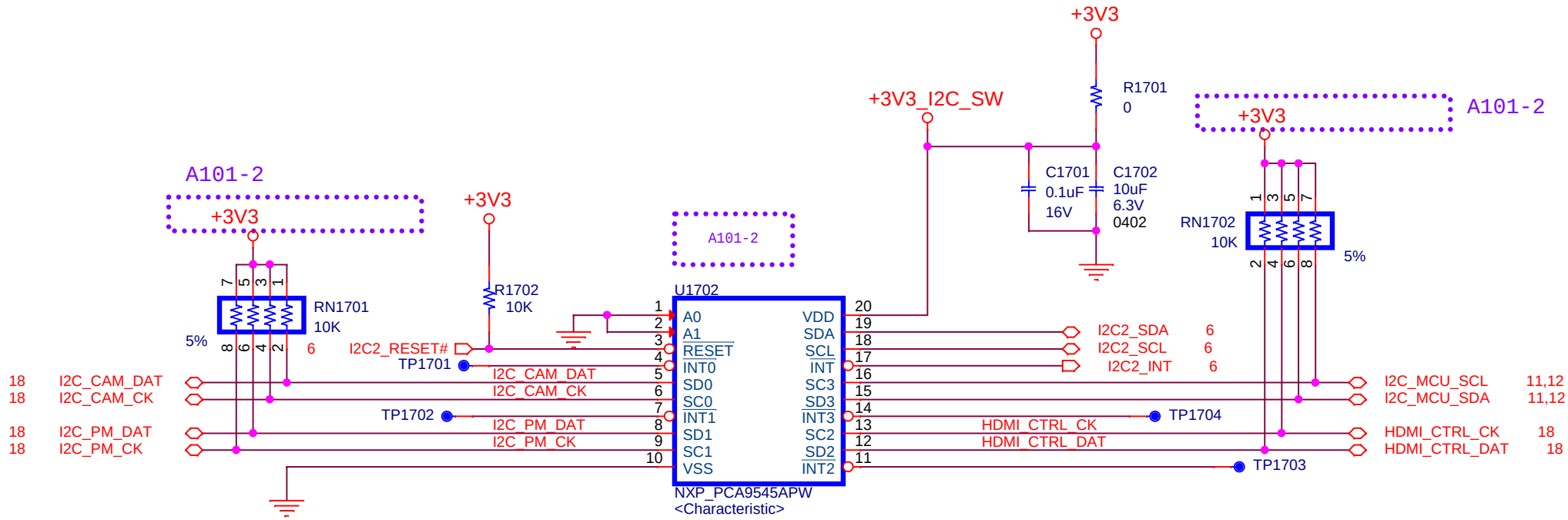
A101-2

+5V @ 0.06A

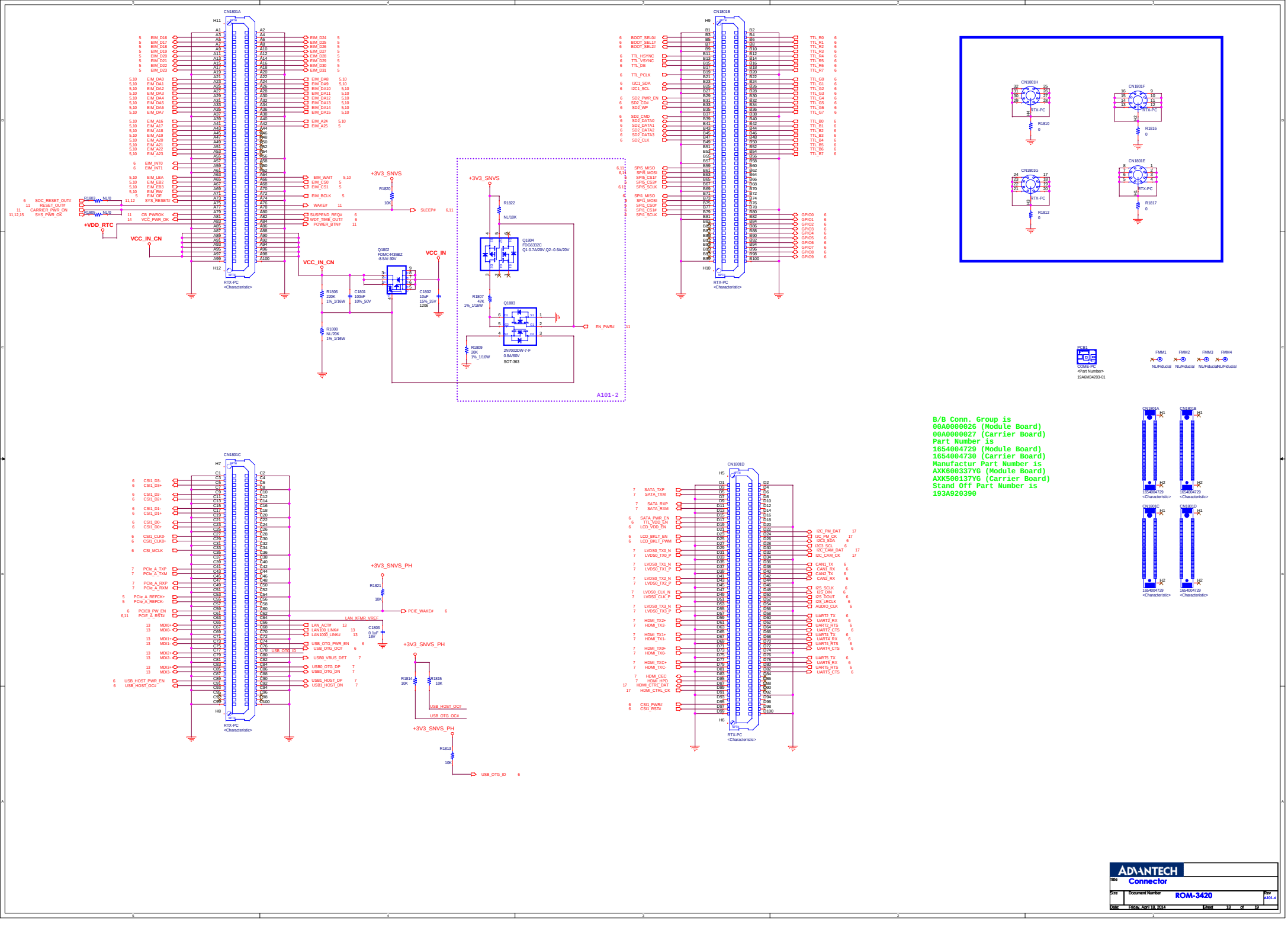
5V Output



Title	DC +5V	
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Title	I2C Switch		
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CN1801A
CN1801B
CN1801C
CN1801D
CN1801H
CN1801F
CN1801G
CN1801E
RTX-PC
<Characteristic>
+3V3_SNVS
+3V3_SNVS_PH
+VDD_RTC
VCC_IN_CN
VCC_IN
Q1802 FDMC4435BZ -8.5A/-30V
Q1804 FDG6332C Q1:0.7A/20V,Q2:-0.6A/20V
Q1803 2N7002DW-7-F 0.8A/60V SOT-363
A101-2
B/B Conn. Group is
00A0000026 (Module Board)
00A0000027 (Carrier Board)
Part Number is
1654004729 (Module Board)
1654004730 (Carrier Board)
Manufactur Part Number is
AXK600337YG (Module Board)
AXK500137YG (Carrier Board)
Stand Off Part Number is
193A920390
PCB1
COME-PC
<Part Number>
19A6M34203-01
FMM1 FMM2 FMM3 FMM4
NU/Fiducial
ADVANTECH
Connector
ROM-3420
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ROM-3420 A101-1 PCB:19A6M34200-01, 96 BOM:9696M34200E Date: 2013/03/08

2013/03/08: Initial Release.

ROM-3420 A101-2 PCB:19A6M34201-01, 96 BOM:9696M34200E Date: 2013/09/17

2013/09/13: CN1801 replace with RTX 2.1 pin define
2013/09/13: Redefine i.MX6 CPU IOMUX. Add systeim bus(EIM). Remove Uart3, SPI4. SPI1 use different GPIO and could not be used as boot rom.
2013/09/17: +5V boost from +3V3
2013/09/17: LAN100_LINK# add a inverter with open-drain output. L1301 replace with 10H. Add C1317, C1318.
2013/09/17: R1503 replace with 6.34K. R1507 replace with 49.9K.
2013/09/17: +3V3_SNVS could go into power saving mode by adding U1405, Q1405. L1401 replace with 3.3uH.
2013/09/17: VCORE_1V4 could go into power saving mode by adding U1406, Q1406.
2013/09/17: MCU U1104 replace with LPC11U14FET48/201. Add C1112.
2013/09/17: Boot strap pull up to +3V3. SPI NOR boot from SPI5. Add R1014.
2013/09/17: B22 replace with 0ohm. NVCC_ENET connects to +3V3 directly. Add C90 10uF.
2013/09/17: I2C pull up to +3V3. ENET_REFCLK add 1uF capacitor in series.
2013/09/17: U1702 change to PCA9545APW.
2013/12/25: L1501 replace with 3.3uH(1211004989-01).
2013/12/25: R1401 stuff and replace with 10Kohm(105A50103A-04).
2013/12/25: C1418 stuff. Q1406 no stuff. R1135 no stuff. R618 stuff. R1150, R1152, R1154 stuff. R1151, R1153, R1155 no stuff.
2013/12/25: R1435, R1438 replace with 1Kohm(105A510014-04).
2013/12/25: U1405 replace with TI_SN74AHCT1G125DCKR(1410021759) and no stuff. U1406 replace with TI_SN74AHCT1G125DCKR(1410021759).
2013/12/25: R1135 no stuff.

ROM-3420 A101-3 PCB:19A6M34202-01, 96 BOM:9696M34200E Date: 2014/03/06

2014/02/13: MCU_RXD & MCU_POR_B swap. MCU_TXD & MCU_SYS_PWR_OK swap. WAKE# connectos to MCU. Add MCU_ID. Add MCU_RESET#.
2014/02/13: U1503 5VIN is powered by +V5LDO_3V3. SYS_PWR_OK PU to +3V3_SNVS.
2014/02/14: Add external RTC chip SEIKO_S-35390A.
2014/02/14: Add C505, C506 for PCIE CLK. C1606 replace with 22uF.
2014/02/27: Del D903. Add Q1406. R1603 replace with 30K ohm.
2014/03/06: Del R1607.

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2014/04/16: EMMC VDDF connects to +3V3. MCU_CARRIER_PWR_ON add PD 10Kohm(R1160).