ADVANTECH

Enabling an Intelligent Planet

AMD HD7750

PCIe® ADD-IN BOARD

Datasheet

(GFX-A3T2-01FST1)

CONTENTS

1. Feature

Model Name	GFX-A3T2-01FST1
Graphics Processing Unit	
GPU	HD7750 (Cape Verde)
Process Technology	28 nm
Graphics Engine Operating Frequency (max)	800 GHz
Form Factor	ATX (168 X 69 mm)
GPU Interface	PCI Express® 3.0 (X16)
Shader Processing Units	512 shaders
Floating Point Performance (single precision, peak)	912 GFLOPs
DirectX® capability	DirectX® 11.1
Shader Model	Shader Model 5.0
OpenGL	OpenGL™ 4.2
OpenCL™	OpenCL™ 1.2
Unified Video Decoder (UVD)	UVD3 for H.264, VC-1, MPEG-2, MPEG-4 part 2 decode
Memory	
Memory Operating Frequency (max)	1125 MHz / 4.5 Gbps
Configuration, type	128-bit wide, 1 GB, GDDR5
Display Interface	
Single / Dual-Link DVI	Dual DVI-D X1
CRT	15-pin D-SUB X 1
HDMI	HDMI X1

2. Functional Overview

2.1. Memory Interface

"Cape Verde (HD7750)" has four DRAM sequencers. Each DRAM channel is 32-bit wide. All DRAM devices must be of the same type, have the same size on each channel, and must run at the same voltage.

Supported DRAM Component Organizations:

- 4, 8, or 16 banks (2, 3, or 4 bank bits). Single- or dual-rank.
- Rows: 1024, 2048, 4096, 8192, 16384, 32768, or 65536 (10, 11, 12, 13, 14, 15, or 16 bits).
- Columns: 256, 512, 1024, or 2048 (8, 9, or 10 bits).
- CS (chip select): 1 or 2.

2.2. Memory Aperture Size

The memory-aperture size can be set up to a recommended maximum of 256 MB through the ROM_CONFIG[2:0] strap or a separate video ROM. Refer to the description of the ROM_CONFIG[2:0] strap in Table 3–36 (p. 52) and the MEM_AP_SIZE [2:0] strap in Table 3–39 (p. 55) for more information.

The memory aperture defines the address range that the CPU can access. The memory-aperture size assigned to the GPU by the system BIOS is different from the physical-memory size that the AMD display driver reports to the operating system and control panel. It does not limit the GPU's ability to use the entire frame-buffer memory at any time. Modern graphics and multimedia applications use drivers to alter the frame-buffer contents—direct manipulation of the frame buffer by the CPU is limited. Therefore, having a memory-aperture size that is smaller than the physical frame-buffer size does not limit performance. The AMD display driver reports the memory size based on the amount of physical VRAM installed on the card rather than the memory-aperture size.

Due to memory-management constraints, the memory-aperture size should be the same as the frame-buffer size for 64 MB, 128 MB, and 256 MB. For frame-buffer sizes larger than 256 MB, such as 512 MB and 1 GB, the memory-aperture size should be 256MB.

2.3. Avivo™ Display System

The AMD Avivo™ display system supports VGA, VESA super VGA, and accelerator mode graphics display on six independent display controllers.

The full features of the AMD Avivo display system are outlined in the following sections.

2.4. DVI/HDMI Features

- Advanced DVI capability supporting 10-bit HDR (high dynamic range) output.
- Supports industry-standard CEA-861B video modes including 480p, 720p, 1080i, and 1080p. For a full list of currently supported modes, contact your local AMD support person.
- Maximum pixel rates for 24-bpp outputs are:
  - DVI—162 MP/s (megapixels per second) for single-link DVI
  - DVI—268.5 MP/s for dual-link DVI
  - HDMI—297 MP/s.
- Compliant with the DVI electrical specification.
- The HDMI specification meets the Windows Vista® logo

2.5. DisplayPort 1.2 Features

- Supports all the mandatory features of the *DisplayPort Standard Version 1.2* and the following optional features on links A, B, C, D, E, and F:
  - ACM packet-type support.
  - ISRC packet-type support.
- Each DisplayPort link can transport up to six video streams; one from each display engine.
- Each DisplayPort link can support three options for the number of lanes and three options for link-data rate as follows:
  - Four, two, or one lane(s).
  - 5.4-, 2.7-, or 1.62-GHz link-data rate per lane.
- Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth.
  - Examples of supported pixel-rate/resolution for four lanes at 5.4-GHz link rate:
    - Link bandwidth allows pixel clocks of up to 718 MP/s for 24 bpp or 574 MP/s for 30 bpp.

- 2560 × 2048 @ 60Hz, 30 bpp is supported.

- Examples of supported pixel-rate/resolution for two lanes at 5.4-GHz link rate:
  - Link bandwidth allows pixel clocks of up to 359 MP/s for 24 bpp or 287 MP/s for 30 bpp.
  - 2560 × 1600 @ 60Hz, 30 bpp is supported.
- The following table shows the maximum pixel rates for four, two, or one lane(s) at 5.4-GHz link rate.

Table 2–4 Maximum Pixel Rates at 5.4-GHz Link Rate

	18 bpp	24 bpp	30 bpp
One Lane	239 MP/s	179 MP/s	143 MP/s
Two Lanes	478 MP/s	359 MP/s	287 MP/s
Four Lanes	957 MP/s	718 MP/s	574 MP/s

- Enhanced audio capabilities:
  - Supports PCM audio rates up to 192 kHz.
  - Dolby-TrueHD bitstream and DTS-HD Master Audio bitstream capable

2.6. Integrated HD-Audio Controller (Azalia) and Codec

- HD-audio HDMI, DisplayPort, and wireless display outputs.
- Multiple output stream DMAs.
- Maximum output bandwidth of 73.728 Mbit/s.
- Low power ECN support.
- Hardware silent stream.
- Function level reset.
- Compatible Microsoft® UAA driver support for basic audio.
- For advanced functionality (as follows), an AMD or a third party driver is required.
- LPCM:
  - Speaker formats: 2.0, 2.1, 3.0, 4.0, 5.1, 6.1, and 7.1
  - Sample rates: 32, 44.1, 48, 88.2, 96, 176.4, and 192 kHz
  - Bits per sample: 16, 20, and 24
- Non-HBR Compressed audio pass-through up to 6.144 Mbps:
  - Supports AC-3, MPEG1, MP3 (MPEG1 layer 3), MPEG2, AAC, DTS, ATRAC, Dolby Digital+, WMA Pro, and DTS-HD.

- HBR compressed audio pass-through up to 24.576 Mbps:
  - Supports DTS-HD Master Audio and Dolby True HD.
- Plug-and-Play:
  - Sink audio format capabilities declaration.
  - Sink information.
  - AV association.
- Lip sync information.
- HDCP content protection

2.7. CRT DAC

- One integrated triple 10-bit DAC with built-in reference circuit, which takes output from either one of the internal display controllers (primary or secondary).
- A single RGB-CRT output.
- Support for the stereo-sync signal to drive a 3D display.
- A maximum pixel frequency of 400 MHz.
- An individual power-down feature for each of the three guns.
- Compliant with the VSIS electrical specification.
- Integrated with a built-in bandgap reference circuitry.
- A static detection circuitry (S_detect) for hot-plug/unplug capability
- An integrated static monitor-detection circuit

2.8. Bus Support Features

- Compliant with the PCI Express® Base Specification Revision 3.0, up to 8.0 GT/s.
- Supports ×1, ×2, ×4, ×8, and ×16 lane widths.
- Supports 2.5 GT/s, 5.0 GT/s, and 8.0 GT/s link-data rates.
- Supports ×16 lane reversal where the receivers on lanes 0 to 15 on the graphics endpoint are mapped to the transmitters on lanes 15 down to 0 on the root complex.
- Supports ×16 lane reversal where the transmitters on lanes 0 to 15 on the graphics endpoint are mapped to the receivers on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports full-swing and low-swing transmitter output levels.

3. PIN Assignment and Description

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	RSVD	Reserved	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock Differential pair
14	HSOp(0)	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSOn(0)		GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0, Differential pair
17	PRSNT#2	Hotplug detect	HSIn(0)	

18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1, Differential pair	RSVD	Reserved
20	HSOn(1)		GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1, Differential pair
22	GND	Ground	HSIn(1)	
23	HSOp(2)	Transmitter Lane 2, Differential pair	GND	Ground
24	HSOn(2)		GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2, Differential pair
26	GND	Ground	HSIn(2)	
27	HSOp(3)	Transmitter Lane 3, Differential pair	GND	Ground
28	HSOn(3)		GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3, Differential pair
30	RSVD	Reserved	HSIn(3)	
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4, Differential pair	RSVD	Reserved
34	HSOn(4)		GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4, Differential pair
36	GND	Ground	HSIn(4)	
37	HSOp(5)	Transmitter Lane 5, Differential pair	GND	Ground
38	HSOn(5)		GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5, Differential pair
40	GND	Ground	HSIn(5)	
41	HSOp(6)	Transmitter Lane 6, Differential pair	GND	Ground
42	HSOn(6)		GND	Ground

43	GND	Ground	HSIp(6)	Receiver Lane 6, Differential pair
44	GND	Ground	HSIn(6)	
45	HSOp(7)	Transmitter Lane 7, Differential pair	GND	Ground
46	HSOn(7)		GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7, Differential pair
48	PRSNT#2	Hot plug detect	HSIn(7)	
49	GND	Ground	GND	Ground
50	HSOp(8)	Transmitter Lane 8, Differential pair	RSVD	Reserved
51	HSOn(8)		GND	Ground
52	GND	Ground	HSIp(8)	Receiver Lane 8, Differential pair
53	GND	Ground	HSIn(8)	
54	HSOp(9)	Transmitter Lane 9, Differential pair	GND	Ground
55	HSOn(9)		GND	Ground
56	GND	Ground	HSIp(9)	Receiver Lane 9, Differential pair
57	GND	Ground	HSIn(9)	
58	HSOp(10)	Transmitter Lane 10, Differential pair	GND	Ground
59	HSOn(10)		GND	Ground
60	GND	Ground	HSIp(10)	Receiver Lane 10, Differential pair
61	GND	Ground	HSIn(10)	
62	HSOp(11)	Transmitter Lane 11, Differential pair	GND	Ground
63	HSOn(11)		GND	Ground
64	GND	Ground	HSIp(11)	Receiver Lane 11, Differential pair
65	GND	Ground	HSIn(11)	
66	HSOp(12)	Transmitter Lane 12, Differential pair	GND	Ground
67	HSOn(12)		GND	Ground
68	GND	Ground	HSIp(12)	Receiver Lane 12, Differential pair
69	GND	Ground	HSIn(12)	

70	HSOp(13)	Transmitter Lane 13, Differential pair	GND	Ground
71	HSOn(13)		GND	Ground
72	GND	Ground	HSIp(13)	Receiver Lane 13, Differential pair
73	GND	Ground	HSIn(13)	
74	HSOp(14)	Transmitter Lane 14, Differential pair	GND	Ground
75	HSOn(14)		GND	Ground
76	GND	Ground	HSIp(14)	Receiver Lane 14, Differential pair
77	GND	Ground	HSIn(14)	
78	HSOp(15)	Transmitter Lane 15, Differential pair	GND	Ground
79	HSOn(15)		GND	Ground
80	GND	Ground	HSIp(15)	Receiver Lane 15, Differential pair
81	PRSNT#2	Hot plug present detect	HSIn(15)	
82	RSVD#2	Hot Plug Detect	GND	Ground

4. Power Consumption

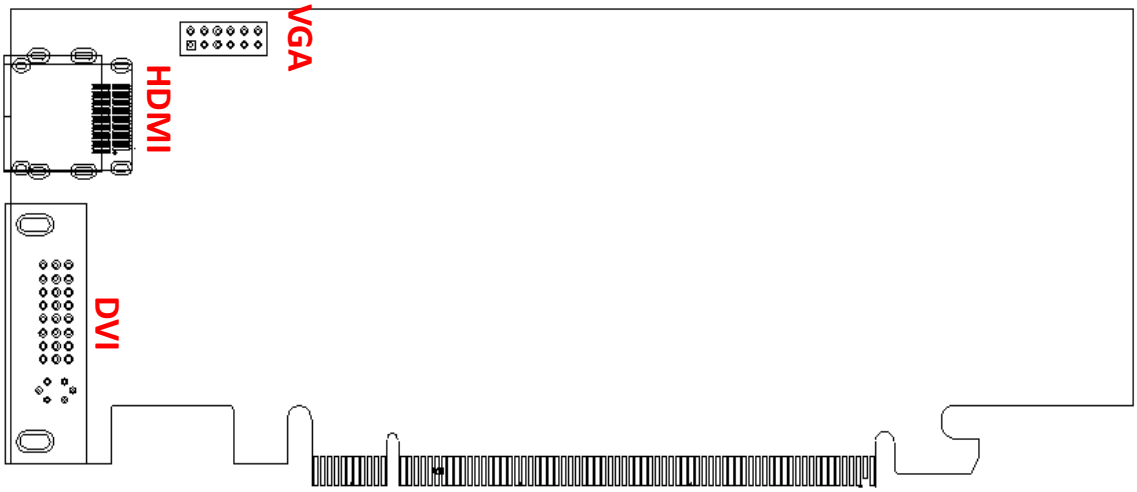
- GFX-A3T2-51FM1

Application	Total ASIC Power + DRAM Power (W)
Static Windows	15.23

Application	Total ASIC Power + DRAM Power (W)
3D Mark Vantage FT6	67.23

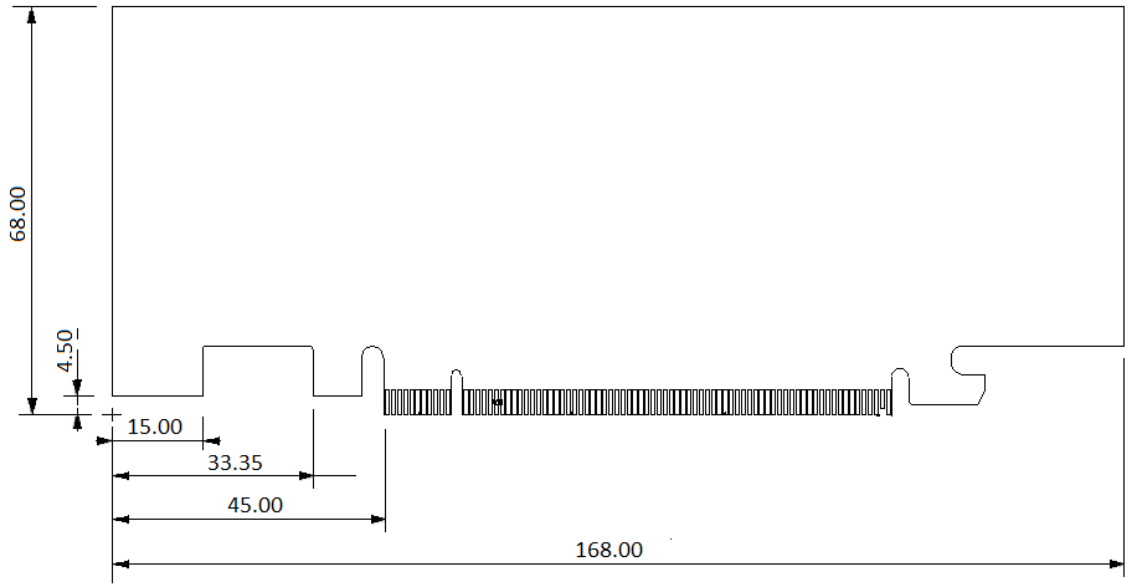
5. Output configuration and Board Dimension

5.1. Output Configuration



5.2 Board Dimension

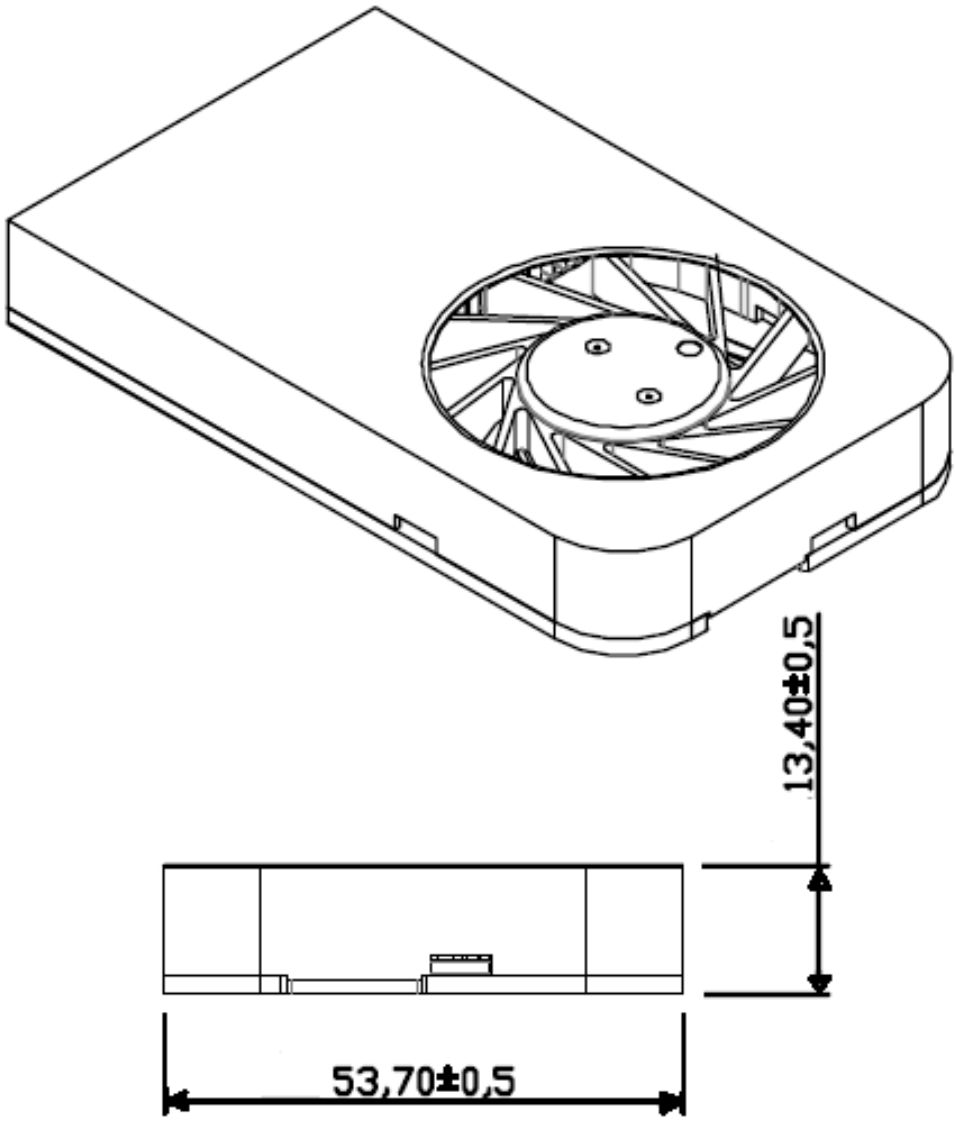
(Unit : mm)

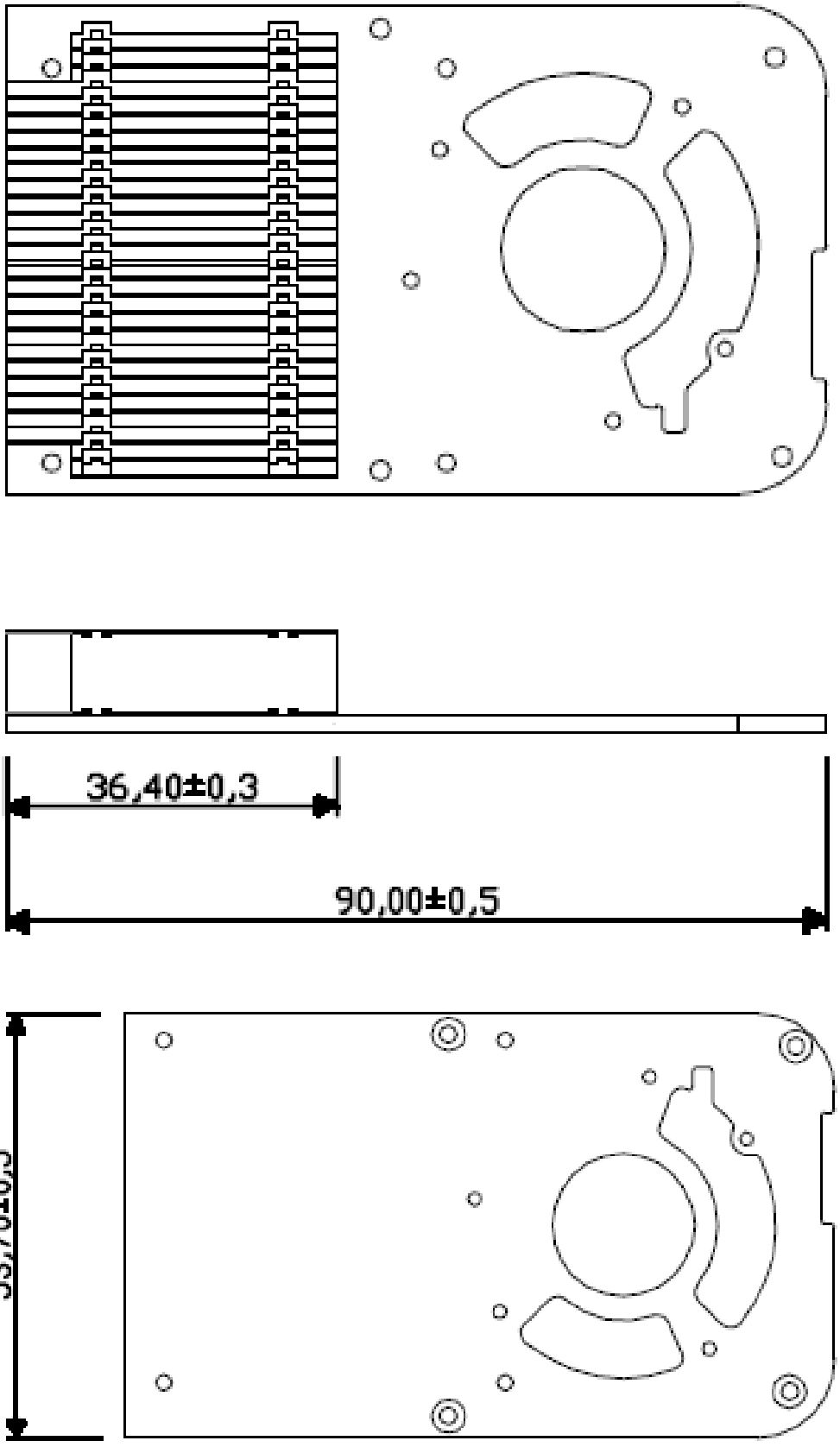


Tolerances : +/_ 0.13 mm

6. Thermal Mechanism

(Unit : mm)

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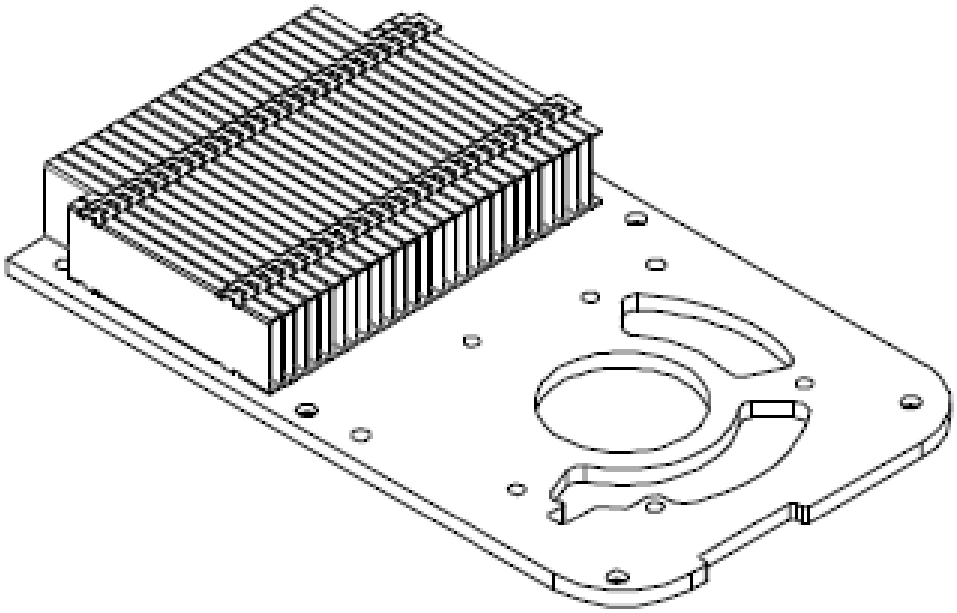

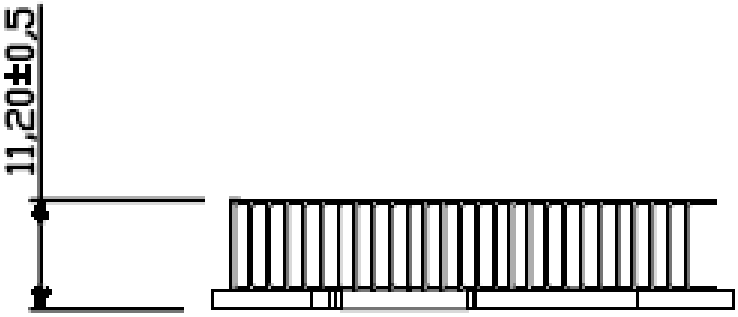
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Change log or update history

Rev.	Data	History
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